Time-Domain Analysis of Transmission Line Circuits

(Part 4)

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Outline

- Reducing undesired transients in TLs with capacitive loads
- Effects of transition times on TL with resistive loads
- Effects of transition times on TL with reactive loads

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Conclusions on Capacitive Terminations

- It is confirmed that lossless TLs with capacitive loads behave as underdriven lines if $R_S > Z_o$
- It is confirmed that lossless TLs with capacitive loads behave as overdriven lines if $R_S < Z_o$
- Undesired transients at the load in lossless TLs with capacitive loads are eliminated if the source is matched
- Undesired transients at the load in lossless TLs with capacitive loads and unmatched source are significantly reduced if a matched resistive load is connected in parallel with the load capacitor (at the expense of more current from the source)

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Effects of t_r on TL with Resistive Termination

- Undesired transients due to fast transition times in lossless TLs with resistive terminations are eliminated if the source, the load, or both, are matched
- If both the source and the load are unmatched, it is confirmed that a significant amount of undesired transients appear when the flight time is larger than 10% of the transition time

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Conclusions on Capacitive Terminations and t_r

- Undesired transients due to fast transition times in lossless TLs with capacitive loads are eliminated if the source is matched
- Undesired transients due to fast transition times in lossless TLs with capacitive loads and unmatched source are significantly reduced if a matched resistive load is connected in parallel with the load capacitor (at the expense of more current from the source)

