Modeling Physical Interconnects

(Part 3)

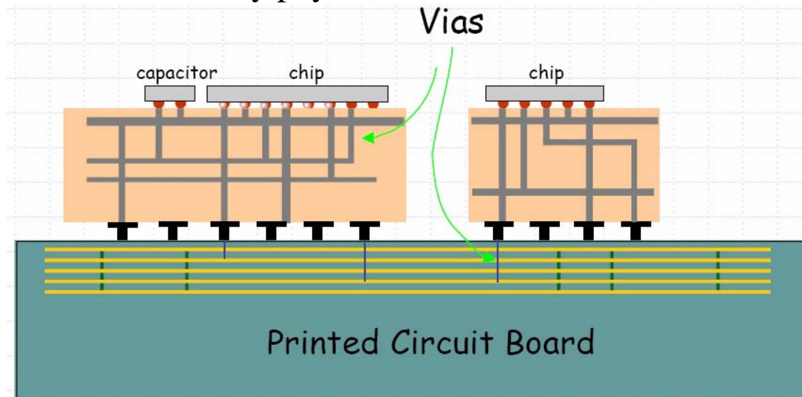
Dr. José Ernesto Rayas Sánchez

Outline

- Vias
- Vias in PCBs
- Types of vias in PCBs
- Pad and antipad
- Nonfunctional pads
- Modeling vias
- Calculating circuit element values with formulas
- Obtaining circuit element values from EM simulations

Vias

- They implement the vertical connections (conductive columns to connect traces on different layers)
- Vias exist at many physical levels:

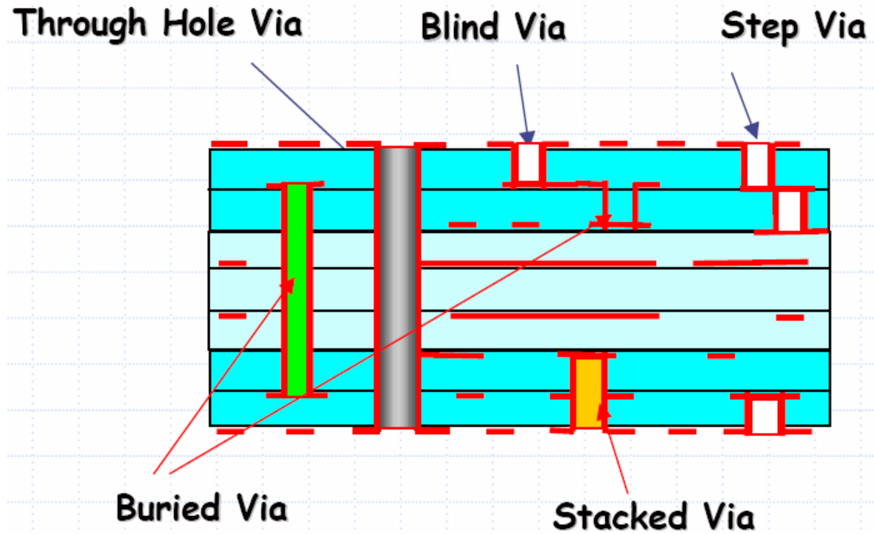


(R. Mellitz, 2003)

Vias in PCBs

- They are formed by drilling a hole (either mechanically or with a laser)
- Blind via: a via not passing through the complete PCB
- Through hole via: a via passing through the entire PCB stackup
- Buried via: a via connecting internal layers
- Conducting vias are "plated" with copper
- Plated through hole (PTH): conductive via passing through the entire PCB stackup

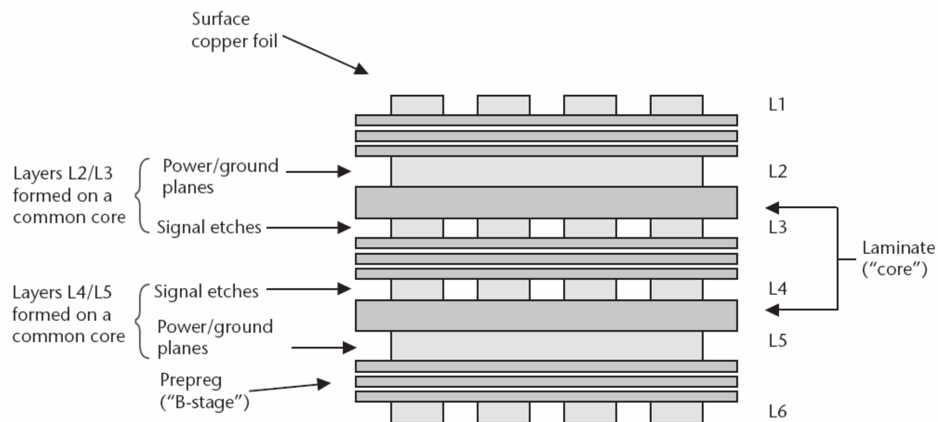
Types of Vias in PCBs



(R. Mellitz, 2003)

PCB Stackup

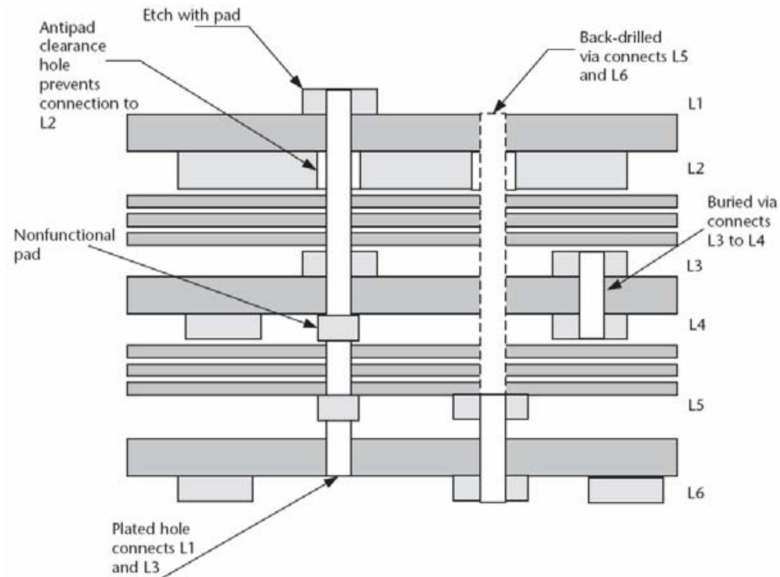
Example showing a 6-layer stackup



(S. C. Thierauf, High-Speed Circuit Board Signal Integrity, Artech, 2004)

Dr. J. E. Rayas Sánchez
http://iteso.mx/~erayas   erayas@iteso.mx

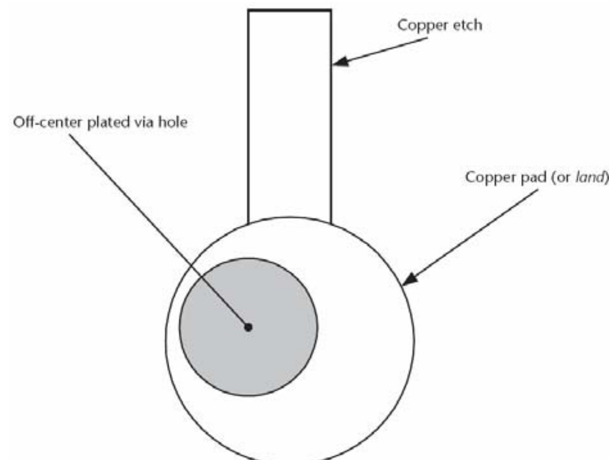
Vias in the PCB Stackup



(S. C. Thierauf, High-Speed Circuit Board Signal Integrity, Artech, 2004)

Pad or Land

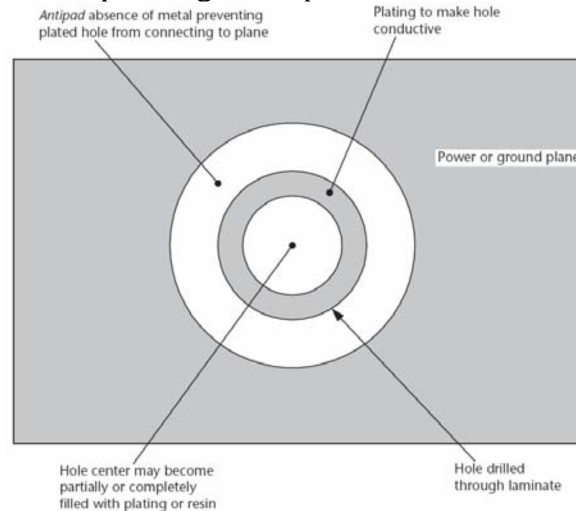
A ring of copper that surrounds a plated via (to ensure electrical contact to traces even if there is some misalignment)



(S. C. Thierauf, High-Speed Circuit Board Signal Integrity, Artech, 2004)

Antipad

A hole in the power/ground plane to avoid electrical contact



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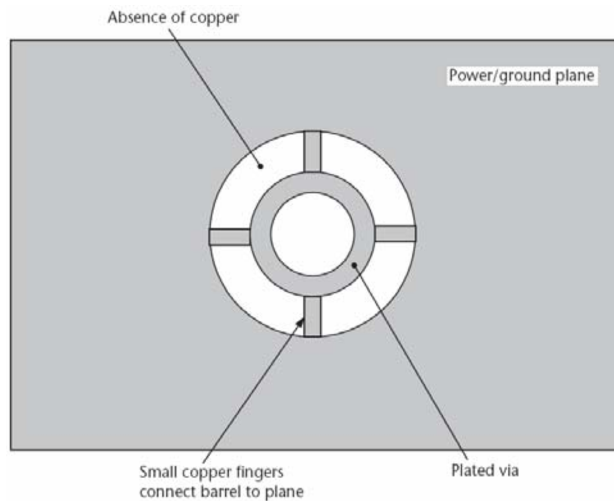
Vias Connecting to Power/Ground Planes

Small copper fingers are used for thermal isolation



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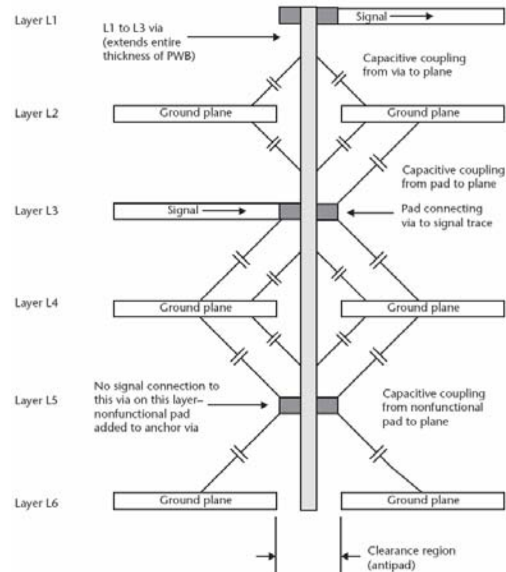
Nonfunctional Pads

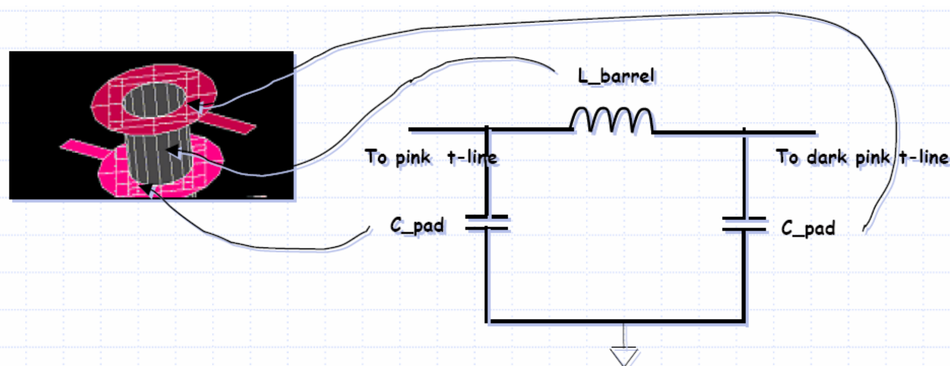
- They are used to anchor the via to the laminate
- ☹ They increase unwanted capacitive coupling to ground/power planes
- ☺ Increasing the antipad decreases the coupling



(S. C. Thierauf, High-Speed Circuit Board Signal Integrity, Artech, 2004)

Modeling Vias

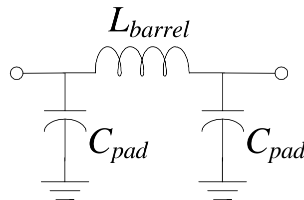
If the via is electrically small (if $t_{d(\text{via})} > 0.1t_t$), it can be modeled with a lumped circuit



(R. Mellitz, 2003)

Modeling Vias (cont)

If the via is electrically small (if $t_{d(\text{via})} > 0.1t_t$), it can be modeled with a lumped circuit



$$L_{barrel} = 5.08h[\ln(4h/d)+1] \text{ (nH)}$$

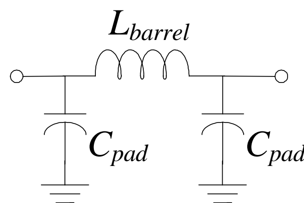
$$C_{pad} = \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1} \text{ (pF)}$$

D_1 : pad diameter (in)
D_2 : antipad diameter (in)
T : thickness of PCB (in)
ε_r: relative permeability of the PCB
h: via length (in)
d: via diameter (in)

Dr. J.E. Rayas Sánchez *(H. Johnson and M. Graham, High-Speed Digital Design, Prentice Hall, 1993)*

Alternative Formula for the Via Inductance

If the via is electrically small (if $t_{d(\text{via})} > 0.1t_t$), it can be modeled with a lumped circuit



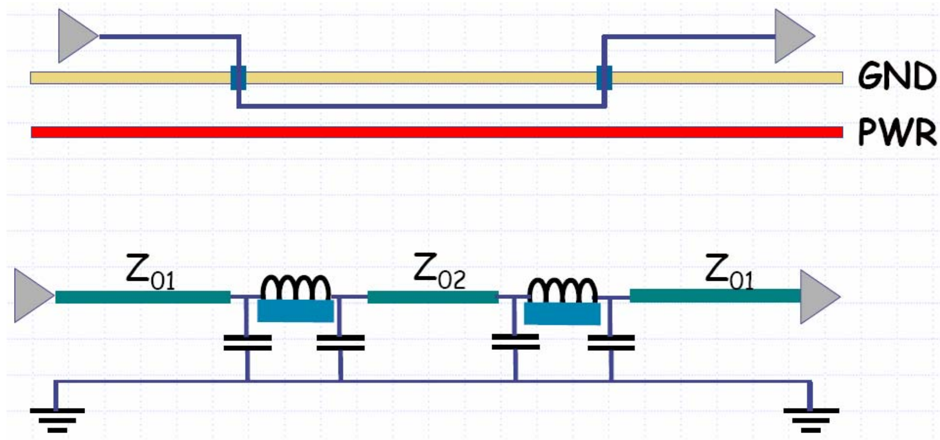
$$L_{barrel} = \frac{\mu_0}{2\pi}\left[h\ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right)+r-\sqrt{r^2+h^2}\right]$$

h: via length (m)
r: via radius (m)

Dr. J.E. Rayas Sánchez *(M.E. Goldfarb and R.A. Pucel, 1991)*

Dr. J. E. Rayas Sánchez
http://iteso.mx/~erayas erayas@iteso.mx

Modeling Vias – Example



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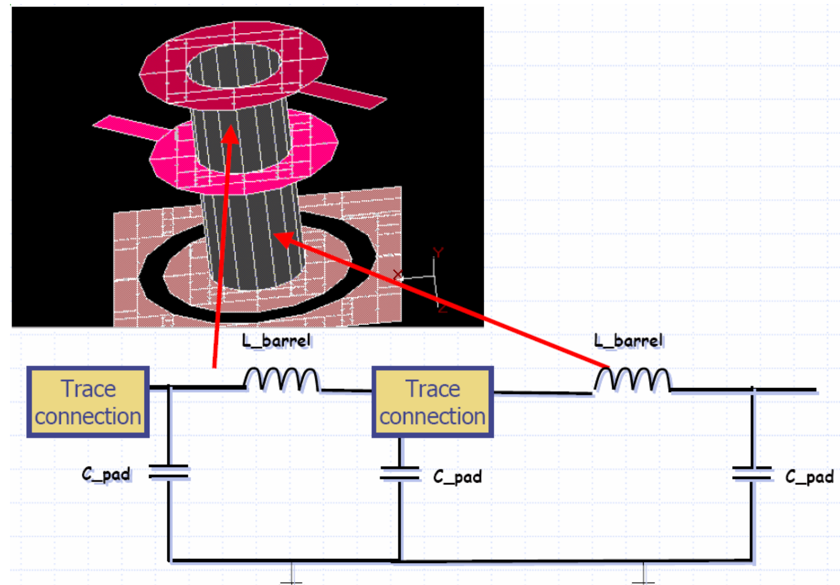
Modeling a Plated Through Hole Via (PTH)



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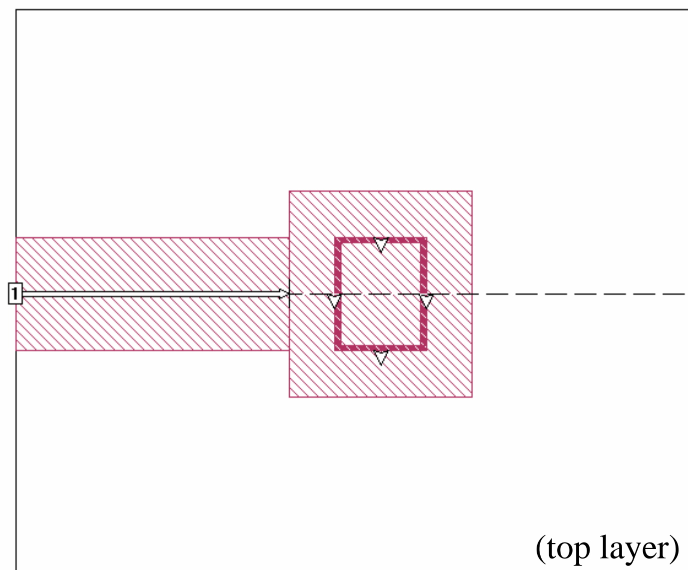
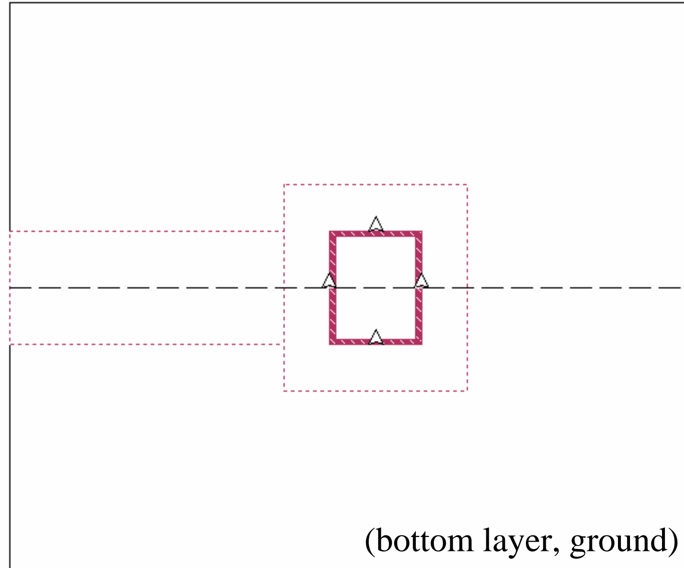
Via Modeling though EM Simulation

- Some electromagnetic simulators have the capability of automatically synthesizing a lumped circuit model using inductors, capacitors, resistors and mutual inductors
- The equivalent circuit is usually provided in SPICE format
- This method is intended for any electrically small circuit (small with respect to the wavelength at the highest frequency of excitation)
- By using this approach, we can develop very accurate models of vias (with arbitrary geometries), without relying on empirical formulas

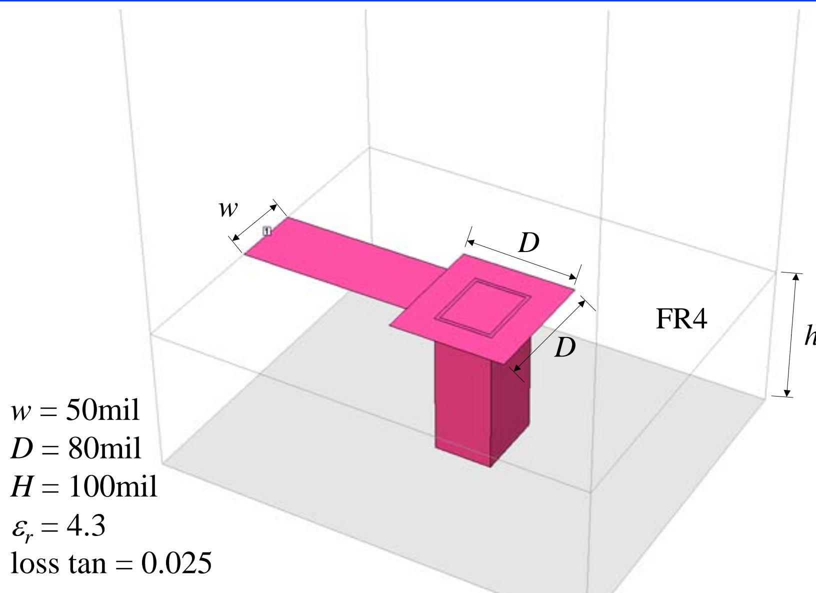
Modeling a Squared Grounded Via Using Sonnet



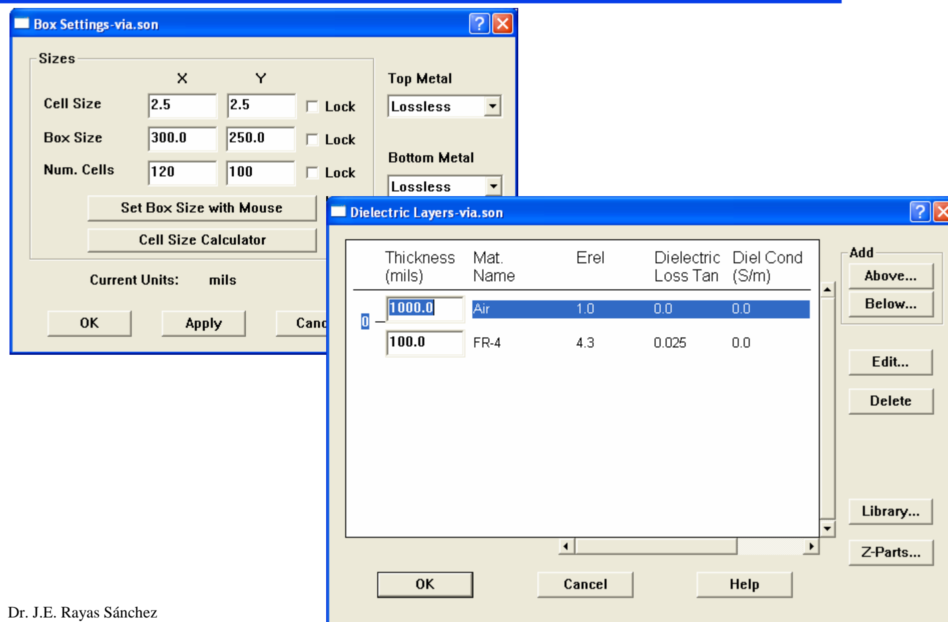
Modeling a Squared Via Using Sonnet (cont)



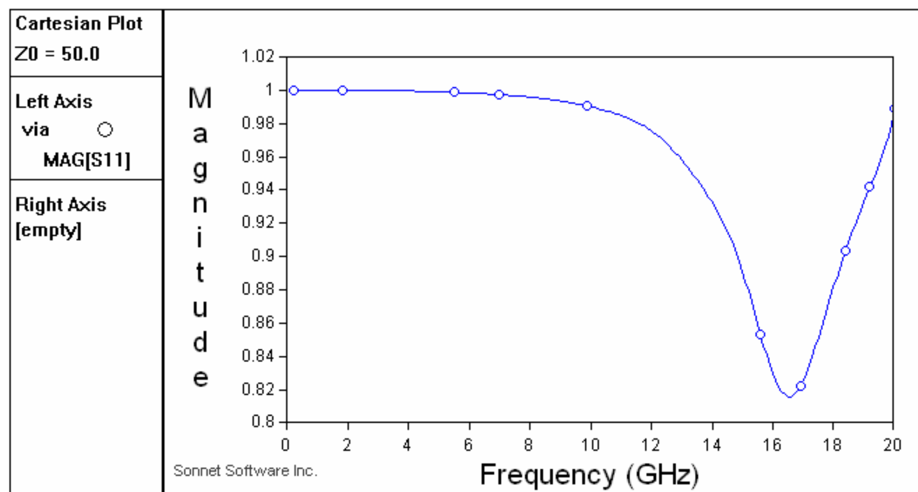
Modeling a Squared Via Using Sonnet (cont)



Modeling a Squared Via Using Sonnet (cont)

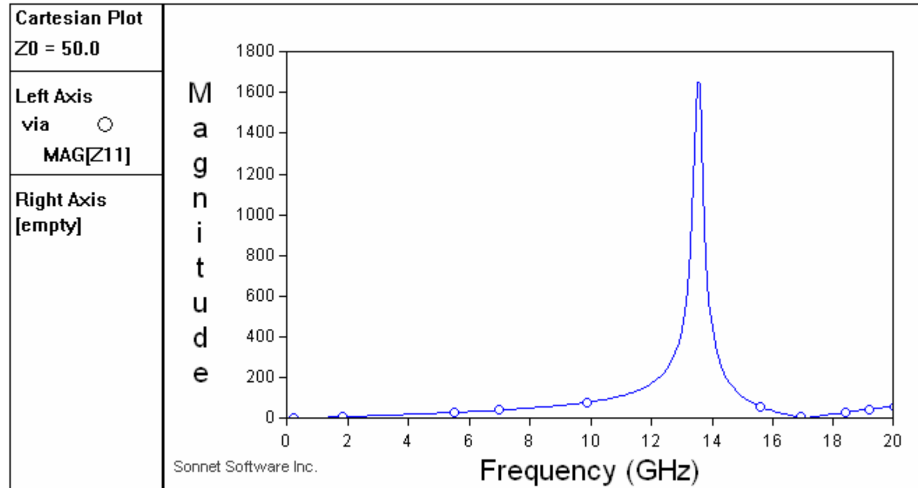


Modeling a Squared Via Using Sonnet (cont)

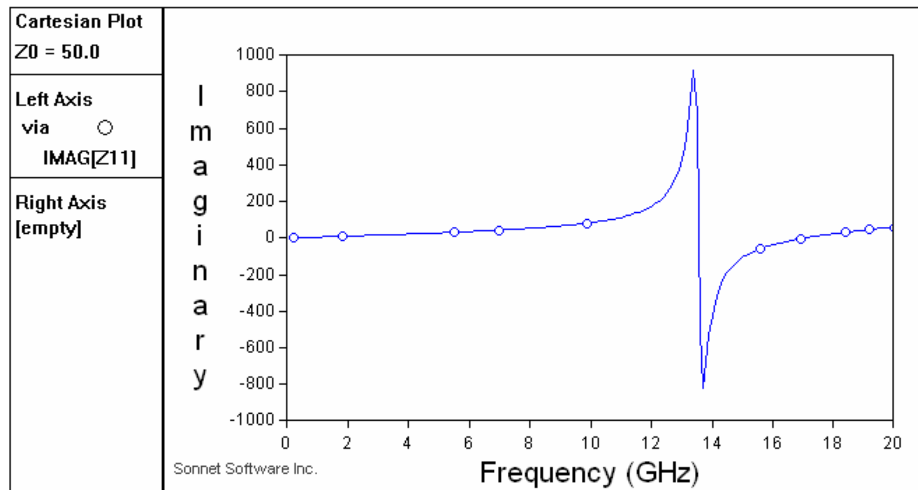


Dr. J. E. Rayas Sánchez
http://iteso.mx/~erayas erayas@iteso.mx

Modeling a Squared Via Using Sonnet (cont)



Modeling a Squared Via Using Sonnet (cont)



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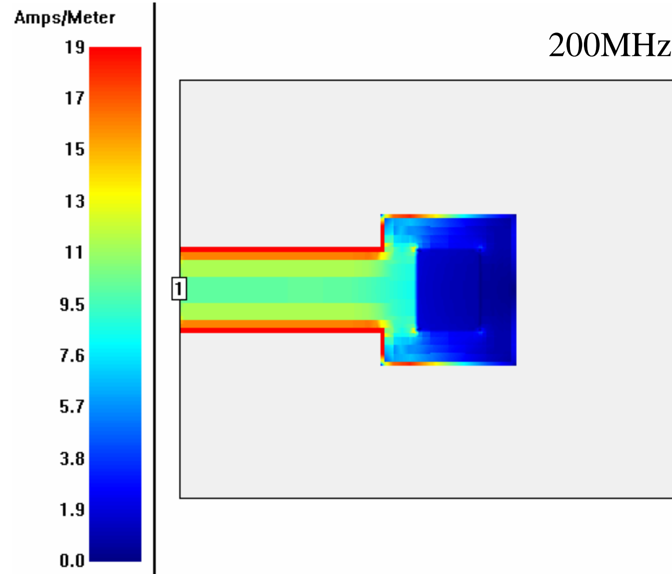
http://iteso.mx/~erayas erayas@iteso.mx

Modeling a Squared Via Using Sonnet (cont)



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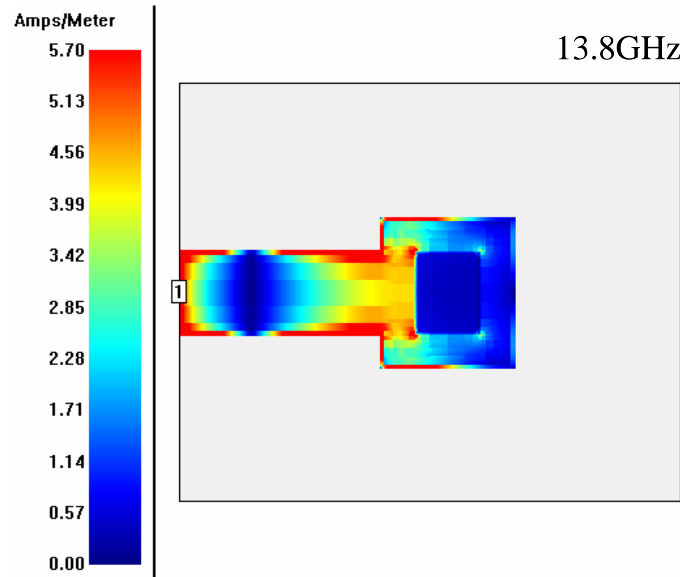
Modeling a Squared Via Using Sonnet (cont)



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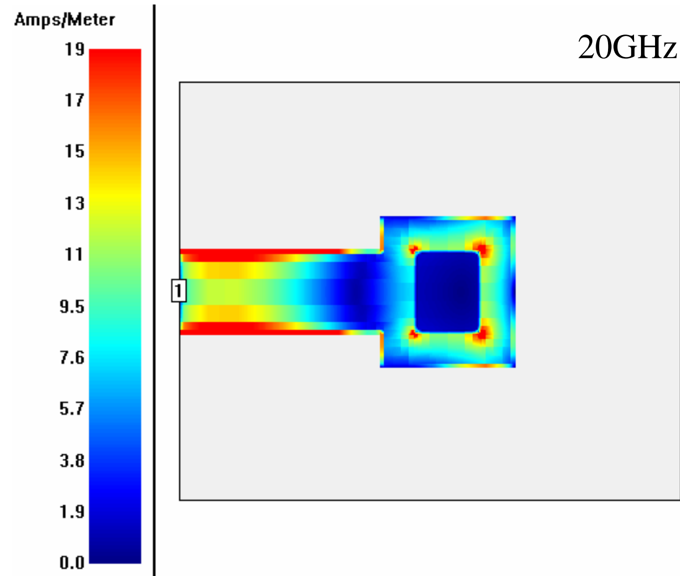
Modeling a Squared Via Using Sonnet (cont)



Modeling a Squared Via Using Sonnet (cont)

emgraph 10.52 - [Output PI Model-via]

File Project Window Help

Format: PSpice   Data Type: De-Embedded   Model Options...

☑ Include Comments   ☑ Include Adaptive Data   ☐ High Precision

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*  From: emgraph Version : 10.52
*  From Emgraph Data: via
*  Data File Written: 05/01/2006 20:50:51
* < HDATE 05/01/2006 20:22:31
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*  Spice Data
* Limits: C>0.01pF L<100.0nH R<1000.0Ohms K>0.01
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L_L1 1 GND 0.809395nh
.ends SON3_0

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R_RL1 2 GND -3.05e-5
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L_L1 1 2 0.808986nh
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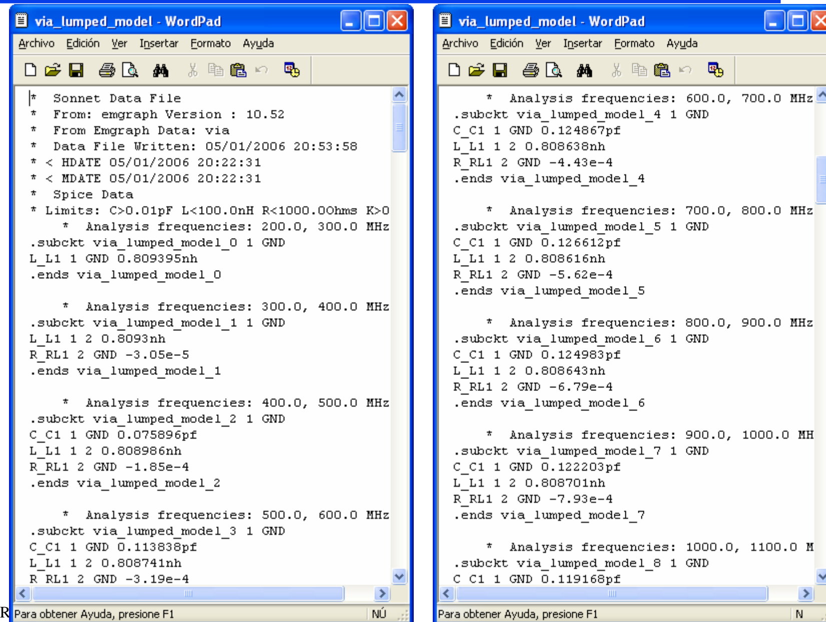
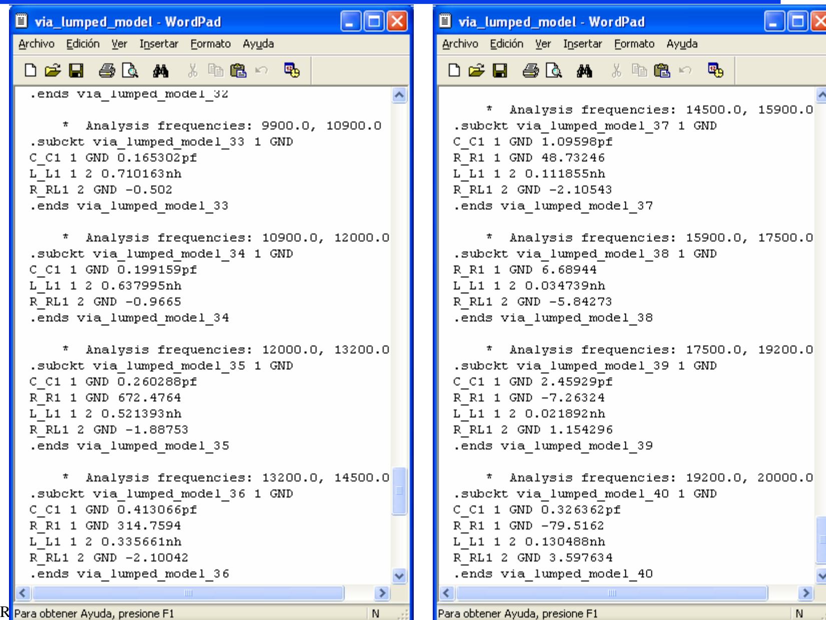
☐ Remember settings   Print   Save...   Close   Help

Modeling a Squared Via Using Sonnet (cont)



Modeling a Squared Via Using Sonnet (cont)



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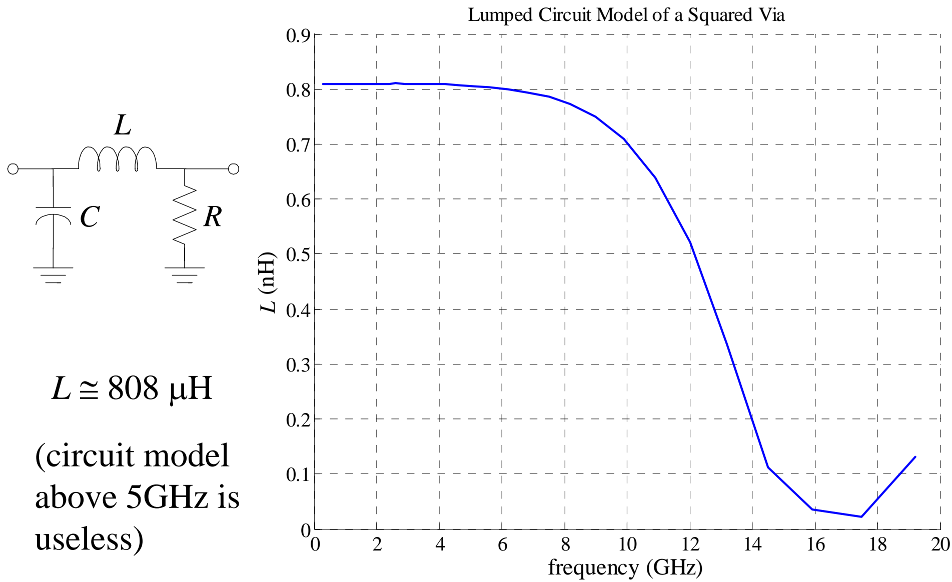
http://iteso.mx/~erayas erayas@iteso.mx

Modeling a Squared Via Using Sonnet (cont)



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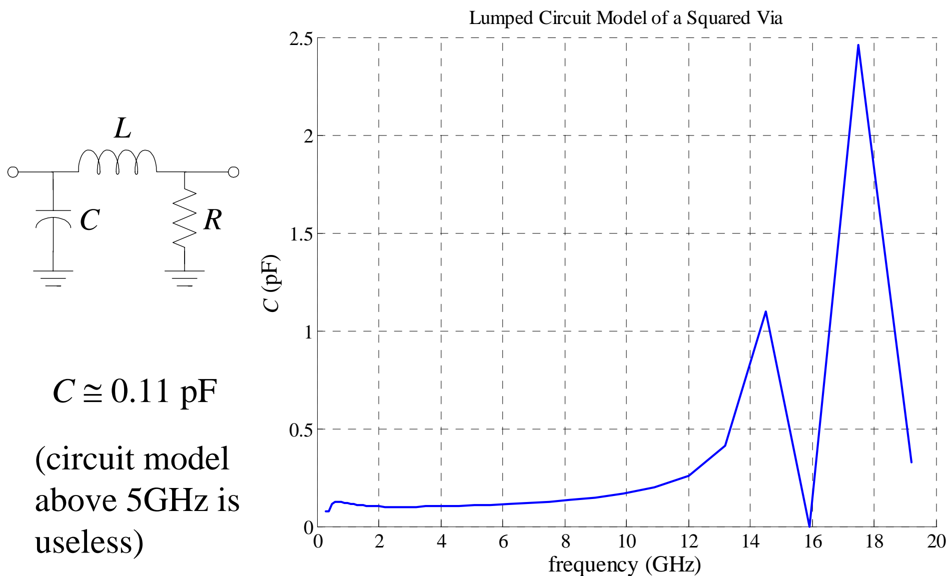
Modeling a Squared Via Using Sonnet (cont)



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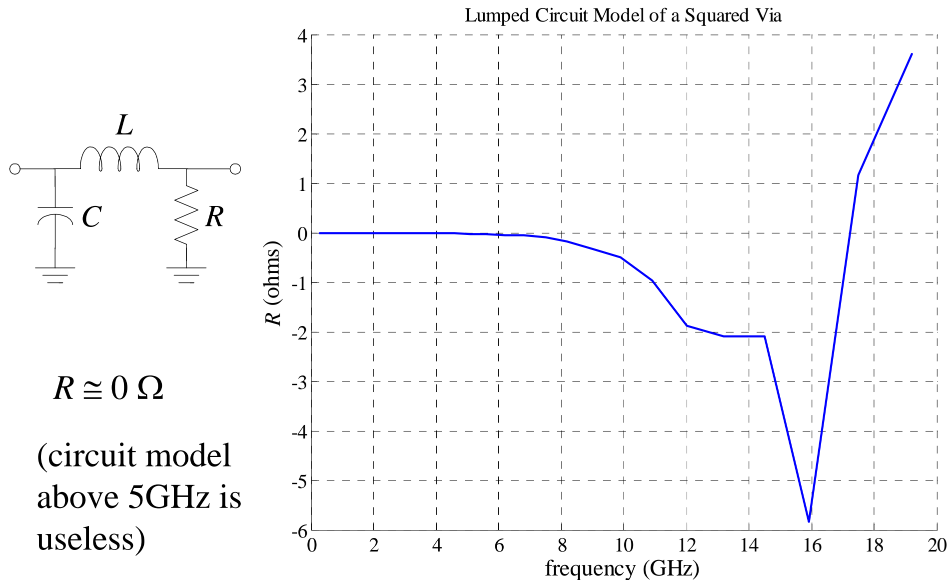
Modeling a Squared Via Using Sonnet (cont)



$R \cong 0\ \Omega$

(circuit model above 5GHz is useless)

Estimating L with Formulas

Taking h = 100mil, d = 50mil

- Using Johnson's formula:

$$L_{barrel} = 5.08h[\ln(4h/d)+1] = 1.5644\ \text{nH}$$

- Using Goldfarb's formula: ($r = d/2$)

$$L_{barrel} = \frac{\mu_0}{2\pi}\left[h\ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right)+r-\sqrt{r^2+h^2}\right] = 0.6675\ \text{nH}$$

Dr. J. E. Rayas Sánchez
http://iteso.mx/~erayas   erayas@iteso.mx