Modeling I/O Buffers

(Part 1)

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Outline

- Buffers driving transmission lines
- Types of buffer models
- Transistor-level models
- Transistor-level models: ECL techniques
- Transistor-level models: GTL techniques

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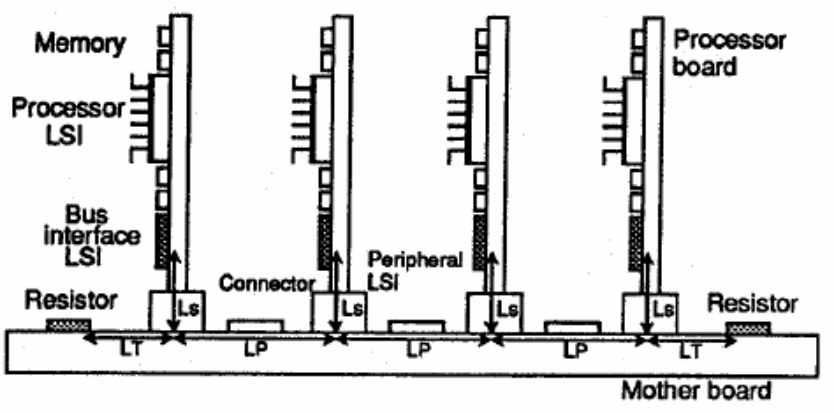
Buffers Driving Transmission Lines

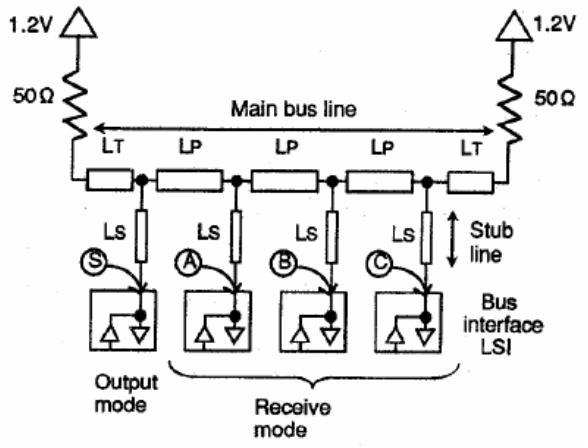
Example of a multiprocessor system



(Kudoh, 1995)

Buffers Driving Transmission Lines (cont)

Bus model of the multiprocessor system



(LP=20cm, LT=10cm, Z0=50ohm)

(Kudoh, 1995)

Types of Buffer Models for Digital Design

- Linear models
- Nonlinear behavioral models
- Detailed electrical models (transistor level)

Transistor Level Models

☺ Advantages
  – Accuracy

☹ Drawbacks
  – Relatively high computational cost during simulation
  – Detailed models are difficult to find (proprietary info)

- Requirements
  – I/O circuit schematic or netlist (text file)
  – Technology process files (foundry)
  – Device dimensions
- Sources of information
  – Component suppliers (databooks, SPICE models)
  – Model libraries from CAD tools

Transistor Level Models – ECL Drivers

- ECL technology allows very high-speed switching
- As oppose to TTL, ECL transistors are not allow to saturate
- ECL buffering techniques are enjoying renewed popularity due to the availability of BiCMOS IC process technology

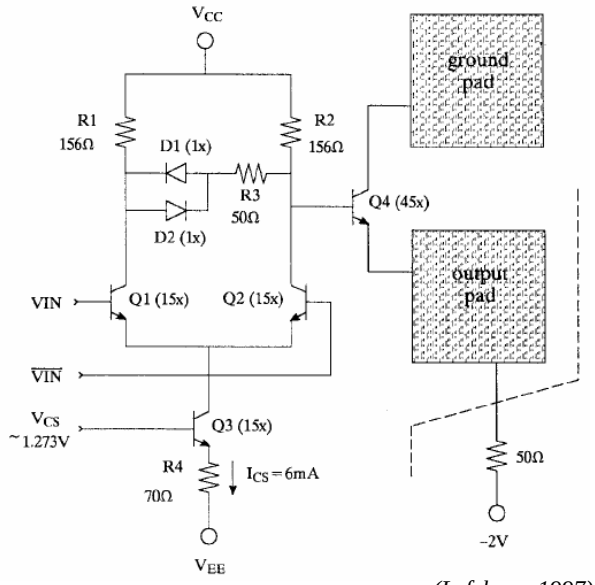
ECL 10K AND 100K LOGIC

	MECL 10K	Fairchild 100K
$V_{OH}(max)$ (V)	–0.81	–0.88
$V_{OH}(min)$ (V)	–0.96	–1.03
$V_{OL}(max)$ (V)	–1.65	–1.62
$V_{OL}(min)$ (V)	–1.85	–1.81

(Lefebvre, 1997)

Transistor Level Models – ECL Drivers (cont)

ECL Output Driver

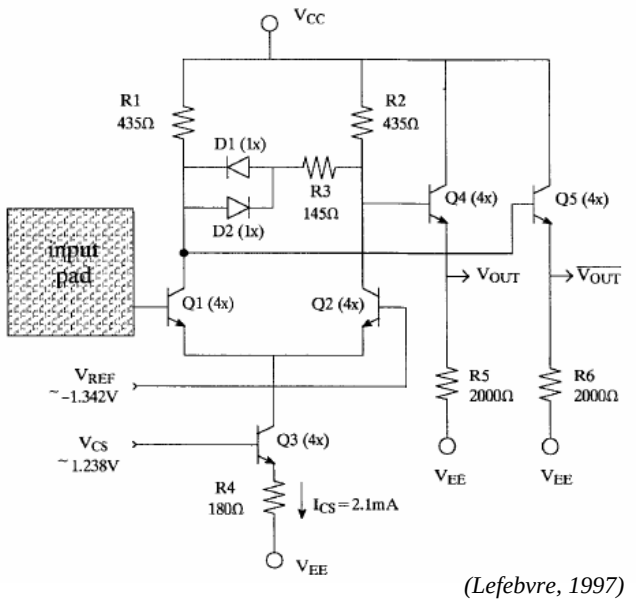


(D_1, D_2 and R_3 are used for temperature compensation)

(Lefebvre, 1997)

Transistor Level Models – ECL Drivers (cont)

ECL Input Driver



(Lefebvre, 1997)

Transistor Level Models – ECL Drivers (cont)

Major drawback of ECL techniques: power consumption

Logic level	Power (Watts)	Termination (both ends)
ECL	20	50Ω to 3.0V
BTL	11	50Ω to 2.0V
GTL	1.5	50Ω to 1.2V

Table 1: Estimated nominal power for 160 active I/O drivers.

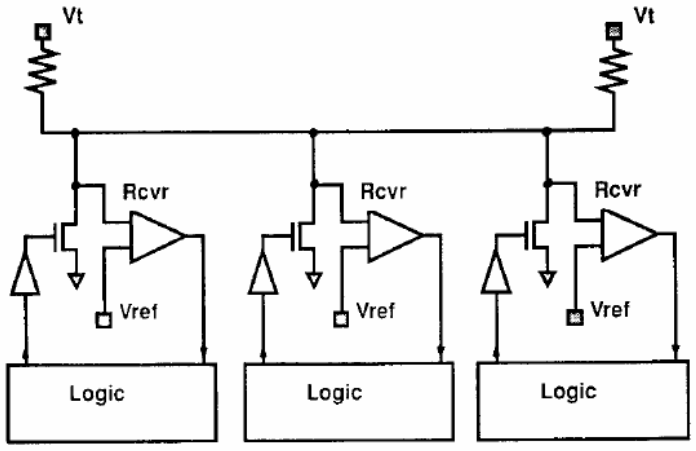
(Gunning, 1992)

Transistor Level Models – GTL Drivers

- GTL uses CMOS process technology (low power consumption and low fabrication cost)
- Essentially, the drivers are open drain NMOS common source stages, and the receivers are NMOS differential amplifiers

Transistor Level Models – GTL Drivers (cont)

I/O Transceivers in a bidirectional transmission line bus



(the transmission line is terminated at both ends)

(Gunning, 1992)

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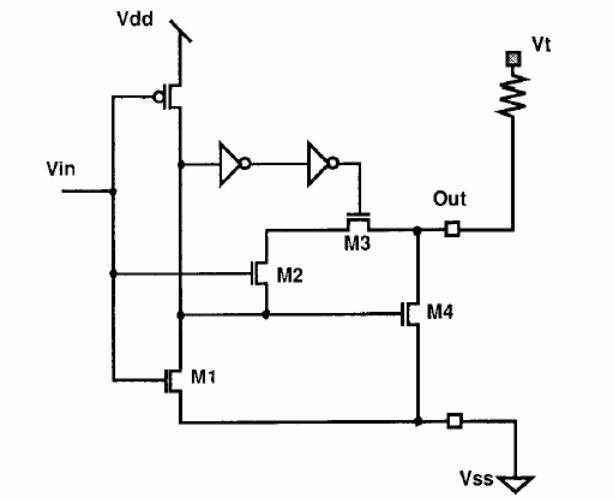
Transistor Level Models – GTL Drivers (cont)

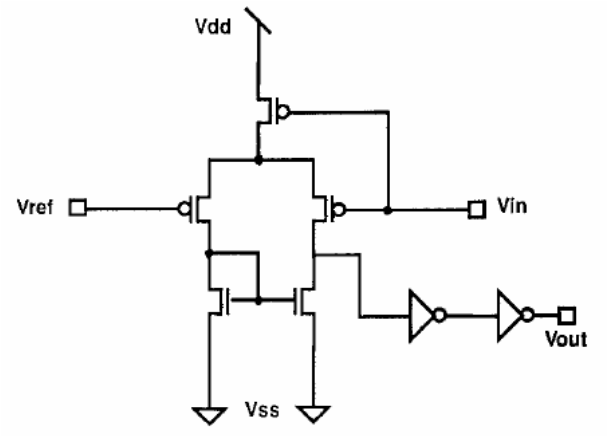
Output driver (transmitter)



(Gunning, 1992)

Transistor Level Models – GTL Drivers (cont)

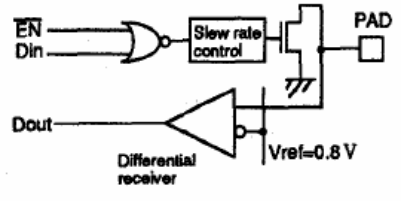
Input buffer (receiver)

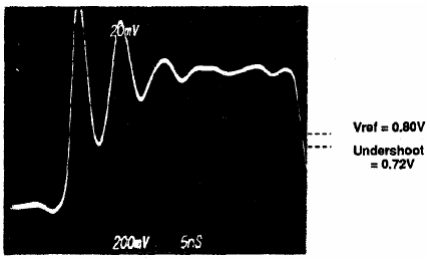


(Gunning, 1992)

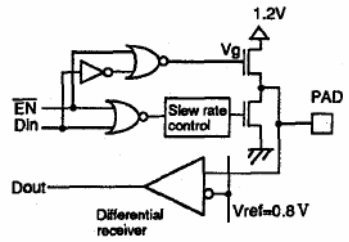
Transistor Level Models – GTL Drivers (cont)

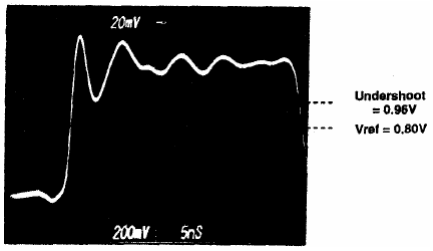
Open drain MOS output driver





Push-pull MOS output driver

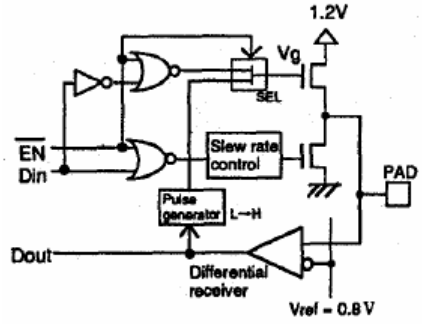


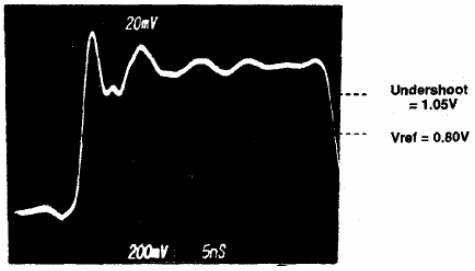


(Kudoh, 1995)

Transistor Level Models – GTL Drivers (cont)

Push-pull MOS output driver with dynamic termination





(In receive mode, the pull-up NMOS transistor acts as a dynamic resistance to compensate the undershoot)

(Kudoh, 1995)