Signal Integrity and High-Speed Interconnects
Assignment 4

May 2006

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Problem 1

A differential trace must be routed through a dense pin field that has a fine pitch. The incoming differential trace has a trace width w = 7mil and a separation d = 14mil (as defined in Fig. 1a). The microstrip traces are on PCL-FR-226 (Polyclad Laminates), with ε_r = 4.5 and loss tangent = 0.019. The substrate height is h = 3.7471mil.

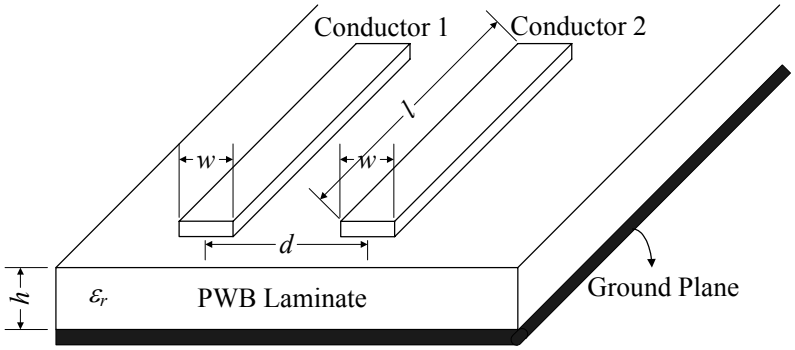


Fig. 1a

The width and spacing of the incoming differential pair must be reduced to pass through the available space left by the antipads, using now w = 4mil and d = 8.5mil, as illustrated in Fig. 1b.

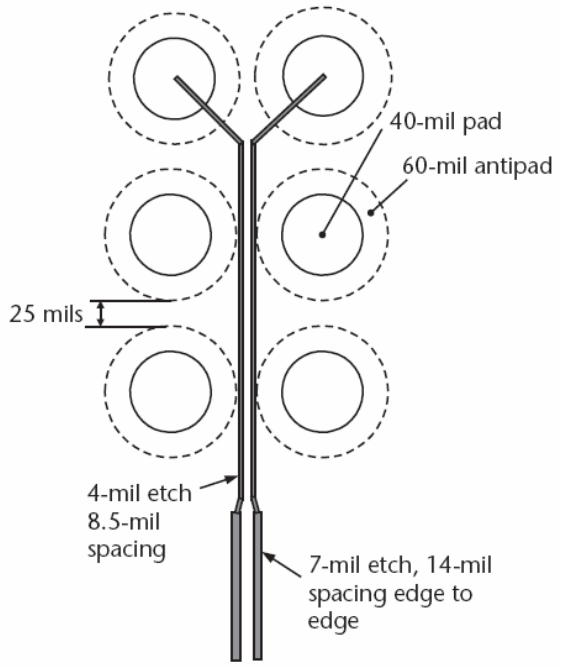
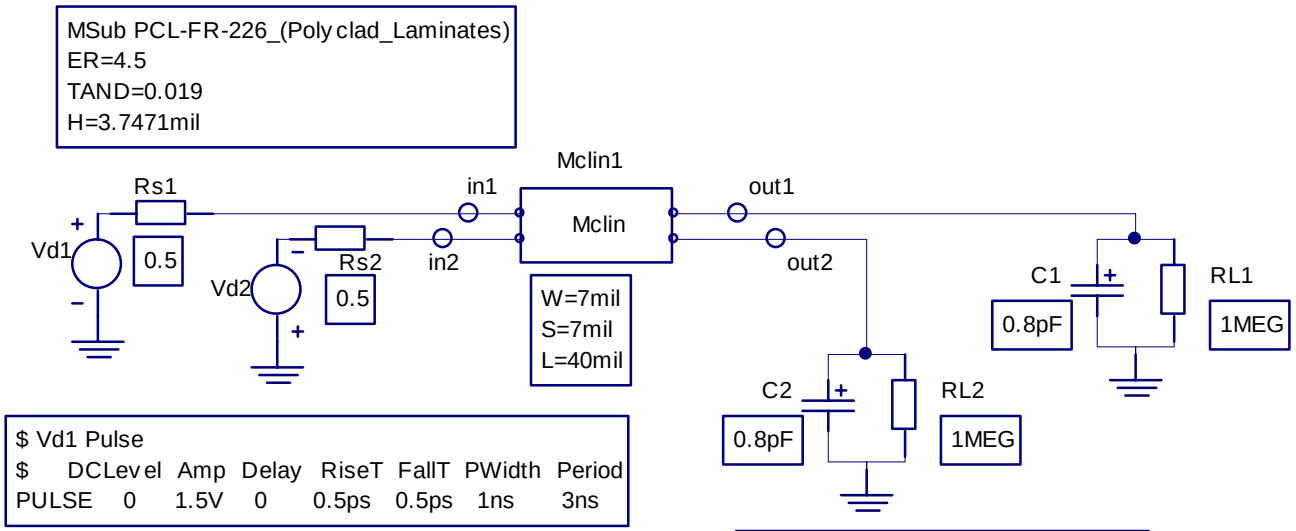


Fig. 1b

a) Considering only the original differential pair (before necking down), calculate the characteristic impedance Z_o of each trace, as well as the characteristic impedance in even and odd modes, $Z_{o\text{-}even}$ and $Z_{o\text{-}odd}$ of the differential trace.

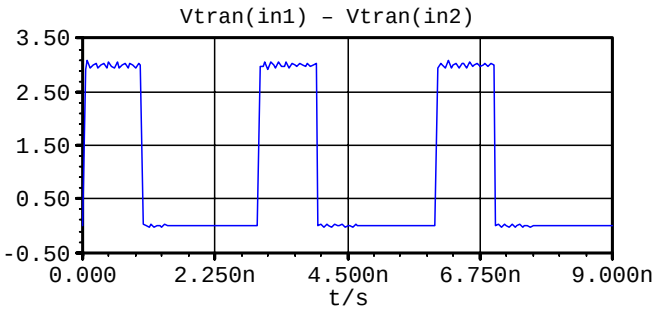
b) Considering the differential pair inside the pin field (after necking down), calculate Z_o, $Z_{o\text{-}even}$ and $Z_{o\text{-}odd}$.

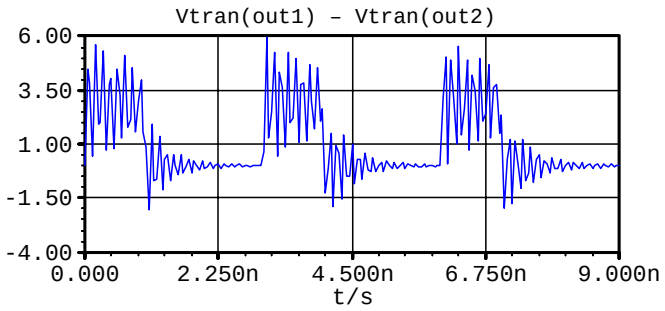
c) Simulate in APLAC the following circuit, which takes into account only the original differential pair (before necking down). The circuit is using the built-in component Mclin available in APLAC for modeling symmetric coupled microstrip lines.



The loads are modeled using typical equivalent circuits for CMOS buffers (the parallel combination of a large resistor and a small capacitance). The source is modeled with an almost ideal linear driver (with an internal resistance of only 0.5Ω).

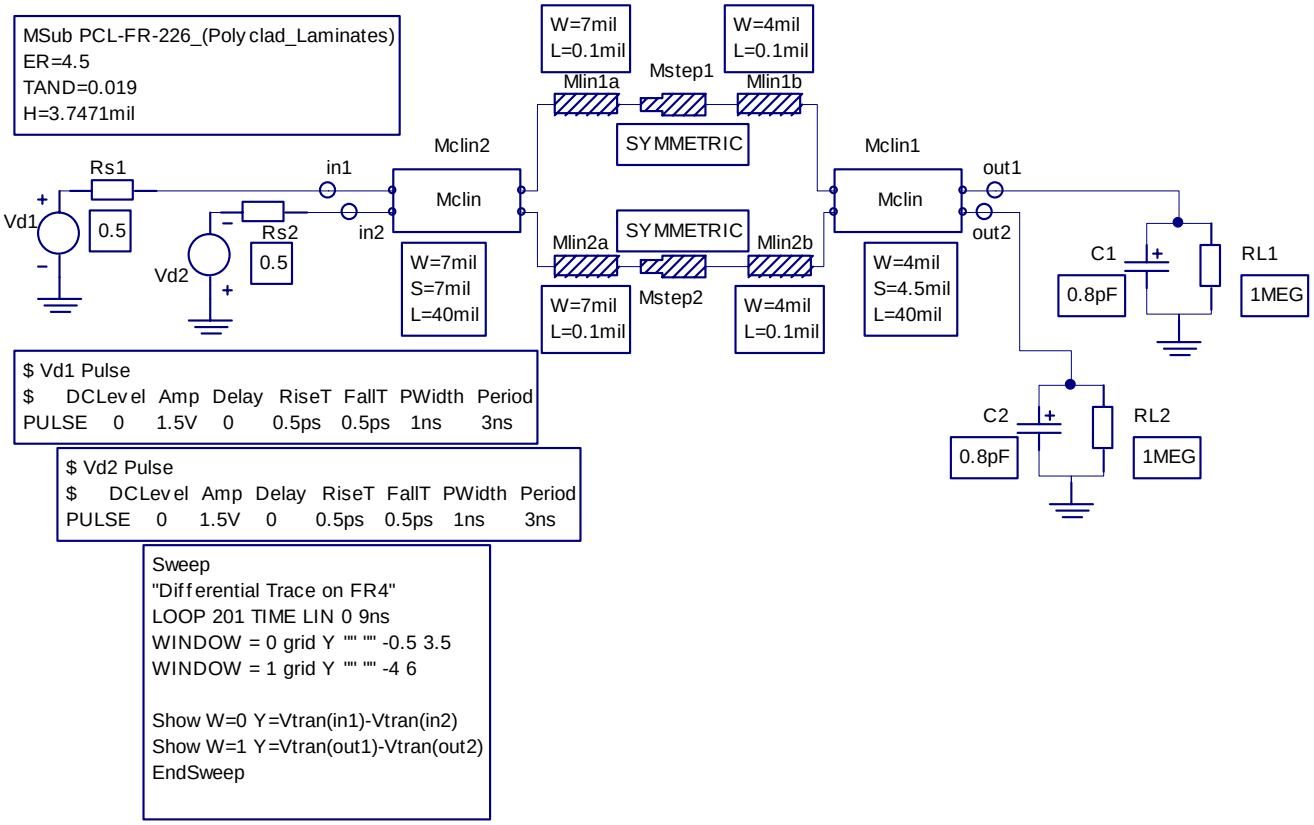
After simulation, you should obtain the following waveforms:



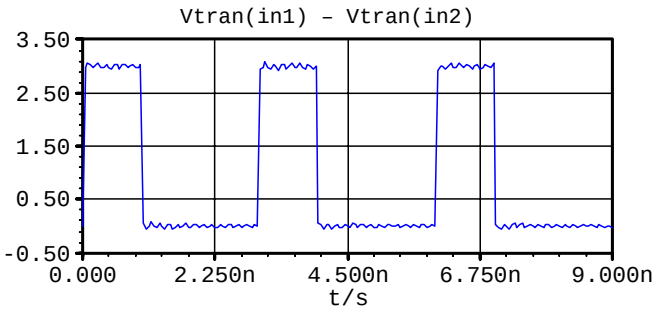


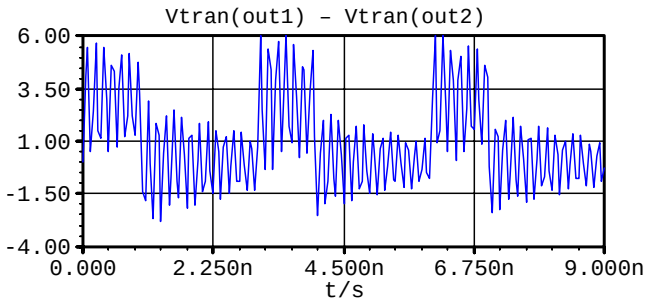
Notice that both the load and the source are unmatched to the differential trace, producing severe multiple reflections in the differential load.

d) Now simulate in APLAC the following circuit, which takes into account not only the incoming differential pair (before necking down) and the differential pair inside the pin field (after necking down) but also the step discontinuity.



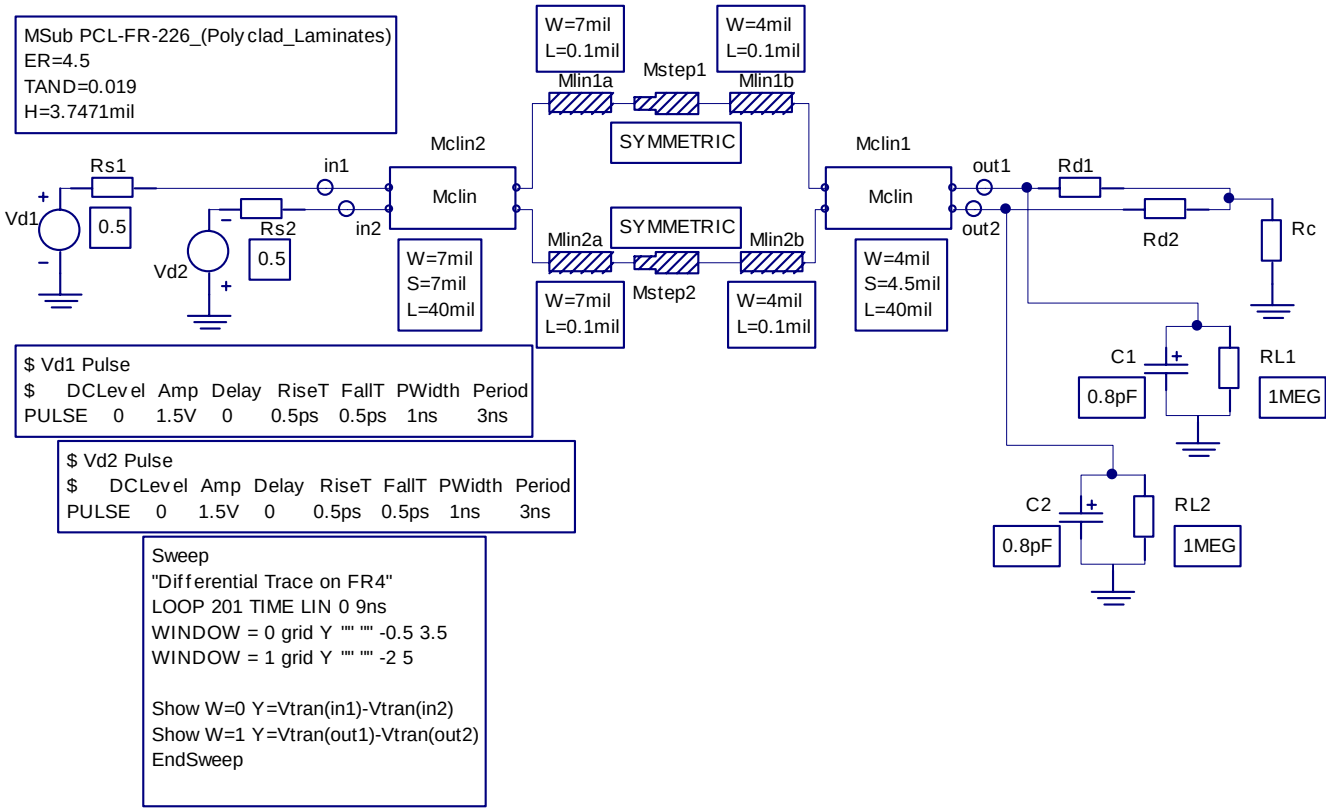
After simulation, you should obtain the following waveforms:



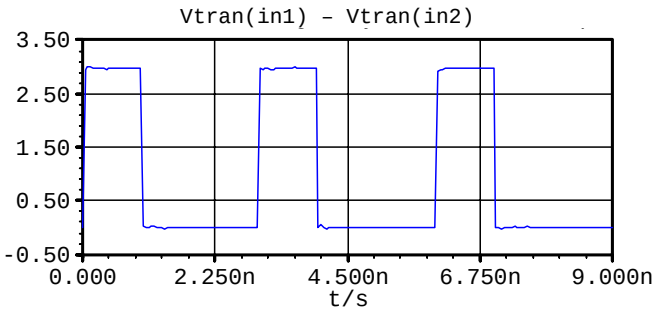


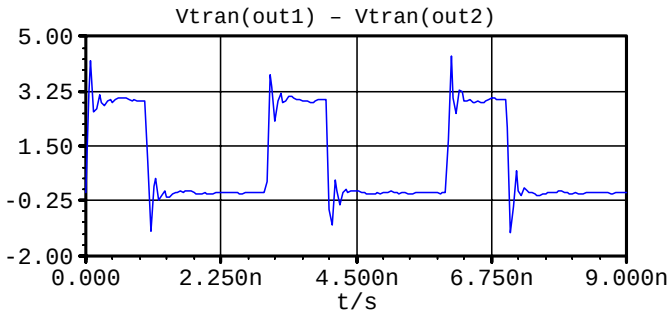
Notice that both the load and the source remain unmatched, producing even larger multiple reflections at output due to the discontinuity in the differential trace.

e) Use the results you obtained in step b) to implement a matched load in parallel to the CMOS buffers, as illustrated in the following circuit. Simulate in APLAC the circuit using the calculated values for $R_{d1} = R_{d2} = R_d$ and R_c.



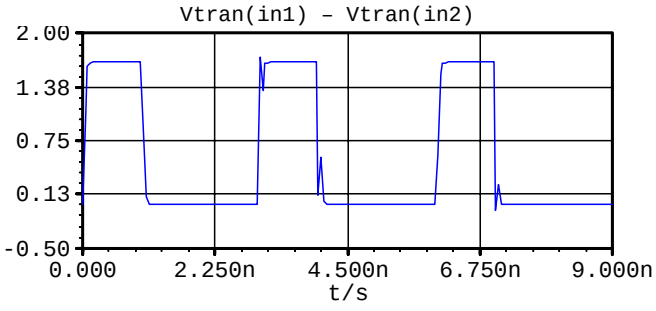
If you properly calculated the values of R_d and R_c, you should be able to obtain the following waveforms:

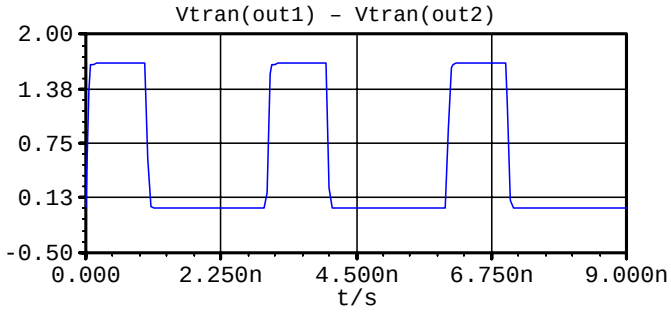




It is seen that signal integrity at the differential input and output improves significantly.

f) Finally, use the results you obtained in the previous step a) to change the values of the internal resistors R_{s1} and R_{s2} (driver's output impedance) to implement a matched source. If R_{s1} and R_{s2} are properly selected, you should be able to obtain the following waveforms:





It is seen that most of the signal integrity problems at the input and output of the differential trace are eliminated by properly matching the source and the load, although there are non-ideal CMOS loads and a discontinuity in the differential trace due to the presence of a dense pin field.

Problem 2

In this problem you will investigate the effects of the power/ground return paths in a multi-layer PCB structure, as well as the effects of the de-coupling capacitors for the power plane. Consider the 3-layer structure shown in Fig. 2a. The signal is transmitted in layer 3 through a stripline trace. Assume $w_1 = w_2 = 100$mil, $W_3 = 3$mil, $h_2 = h_3 = 6$mil, and $\varepsilon_{r2} = \varepsilon_{r3} = 4.4$ (uniform dielectric for the stripline). The top layer will be neglected ($h_1 = \infty$, $\varepsilon_{r1} = 1$). The length of the multi-layer structure is 50mil.

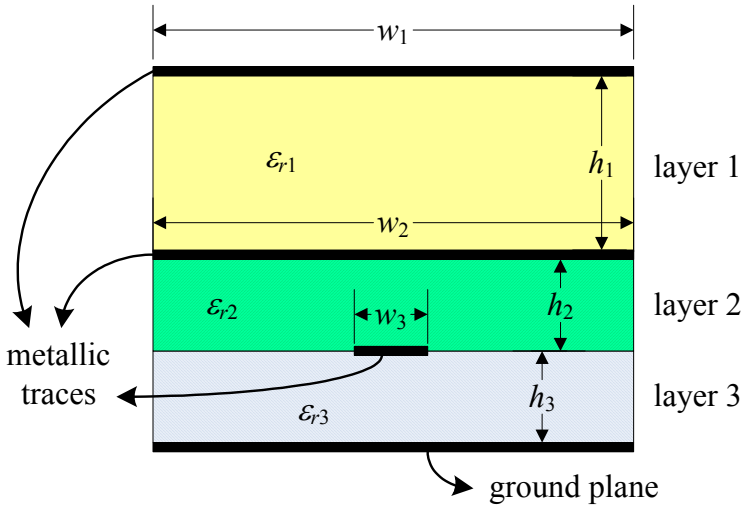


Fig. 2a

The signal driver will be modeled as a quasi-linear buffer (see Fig. 2b), using $V_{DD} = 3.3$V. Initially, $R_{on} = 55\Omega$ and $R_{off} = 45\Omega$. You will later modify the values of R_{on} and R_{off} to improve the signal integrity.

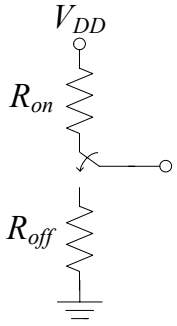
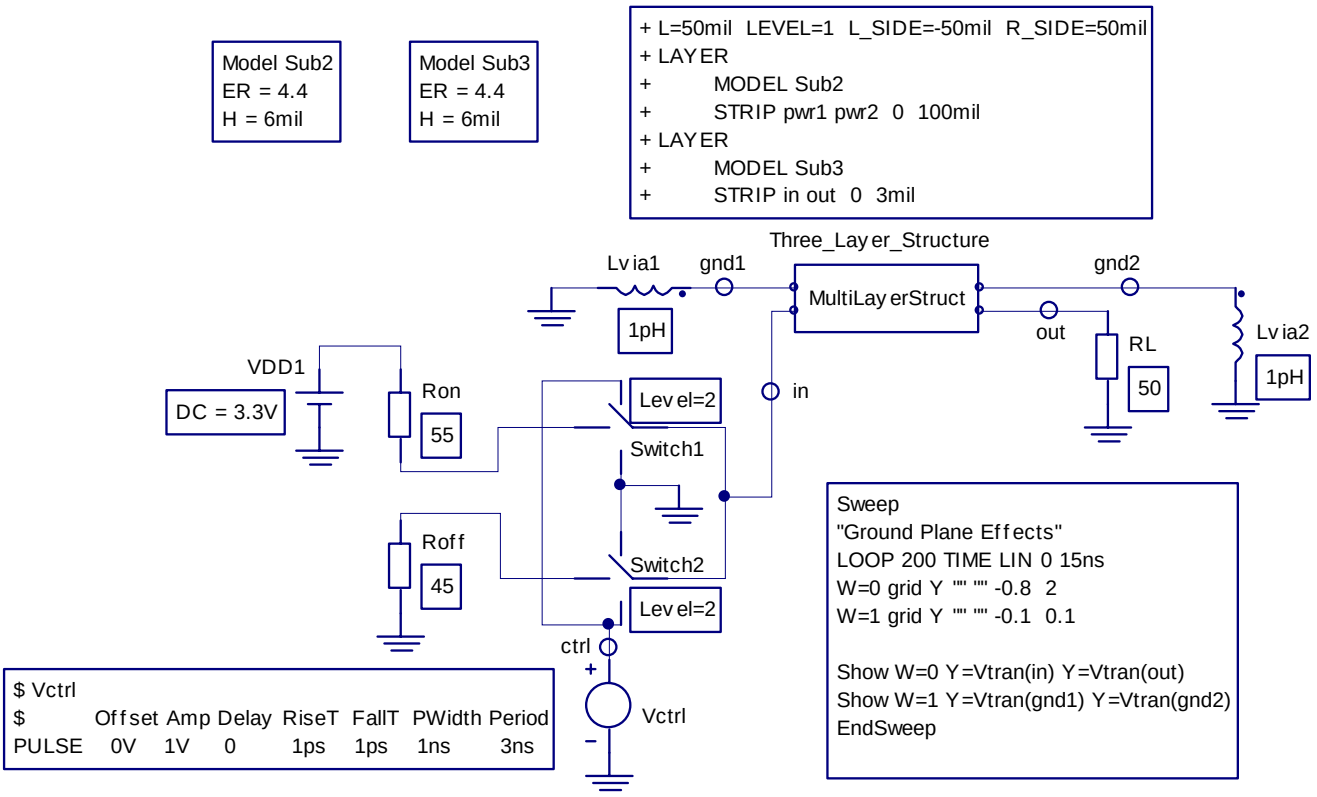
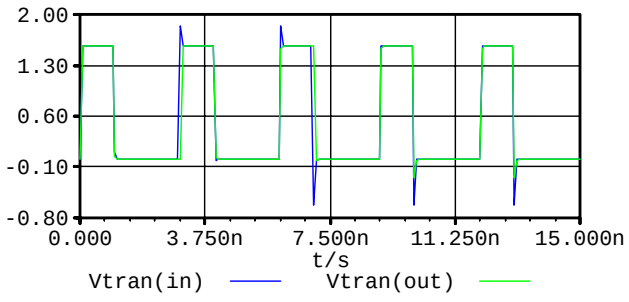


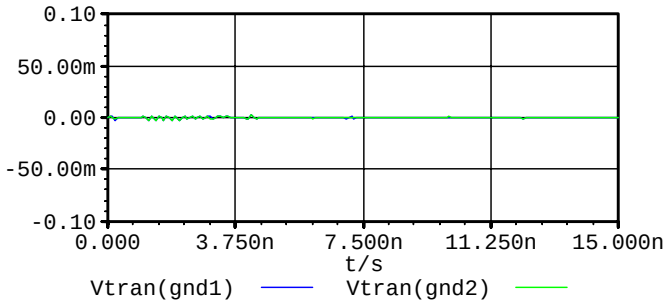
Fig. 2b

a) Simulate the following circuit in APLAC, which represents the case when two grounded planes are used as return paths. Notice that the connection to the upper ground plane is realized through vias modeled by ideal inductors of 1pH each. The circuit is using the built-in component MultiLayerStruct available in APLAC to implement the 3-layer structure (the top layer, layer 1, is made of air and it is infinitively thick).

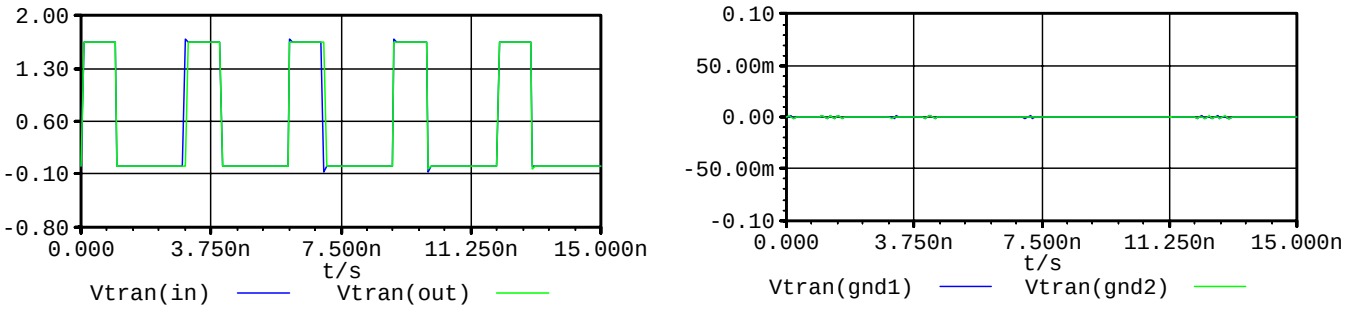


After simulation you should obtain the following waveforms. It is seen that we have some reflections at the input and output of the signal path, and the return path (upper ground plane) is quite.



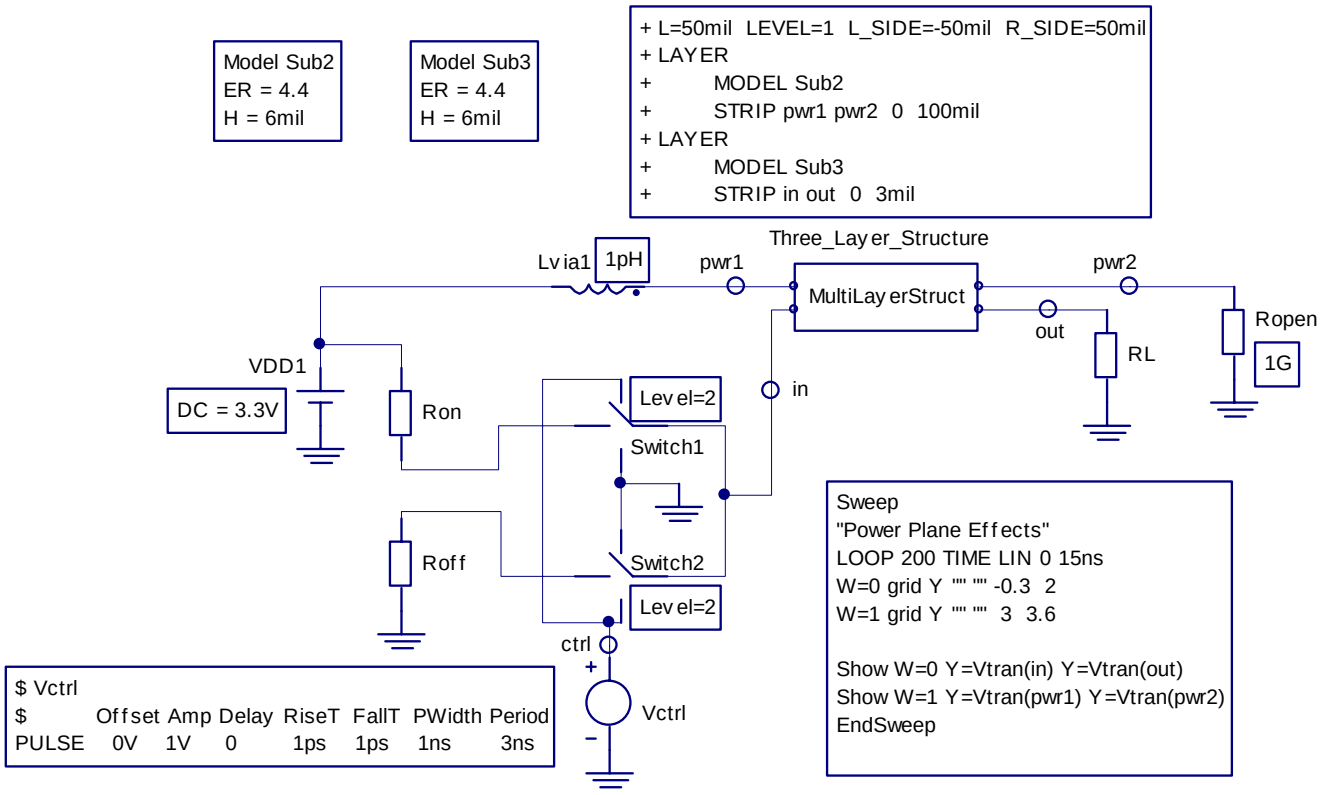


b) Calculate the characteristic impedance Z_o of the signal trace (stripline). Simulate again the previous circuit in APLAC but now making $R_{on} = R_{off} = R_L = Z_o$. If Z_o is properly calculated, you should be able to obtain the following waveforms:

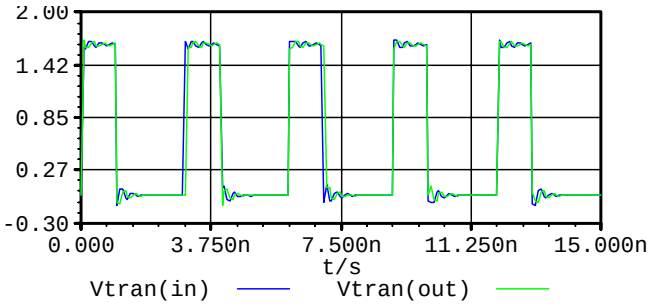


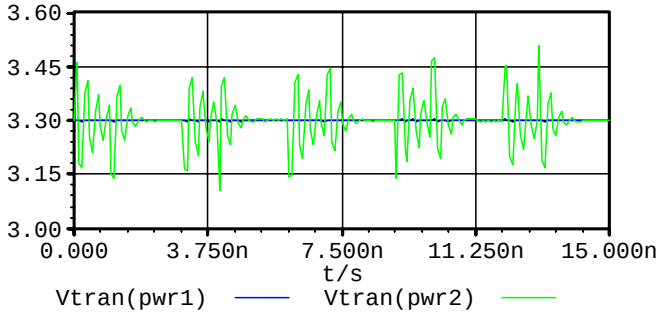
Notice that most of the signal integrity problems in the signal path have been eliminated, and that the upper return grounded plane is still quite.

c) Now you will connect the metallic plane above the signal trace to the DC voltage source, and simulate again the circuit in APLAC, as shown below. In this case, the metallic plane above the signal trace is used as a power plane. The connection to the power plane is realized through a via, as indicated in the schematic. The power plane is left open at the end of the signal trace (this open circuit is modeled using $R_{open} = 1\text{G}\Omega$).

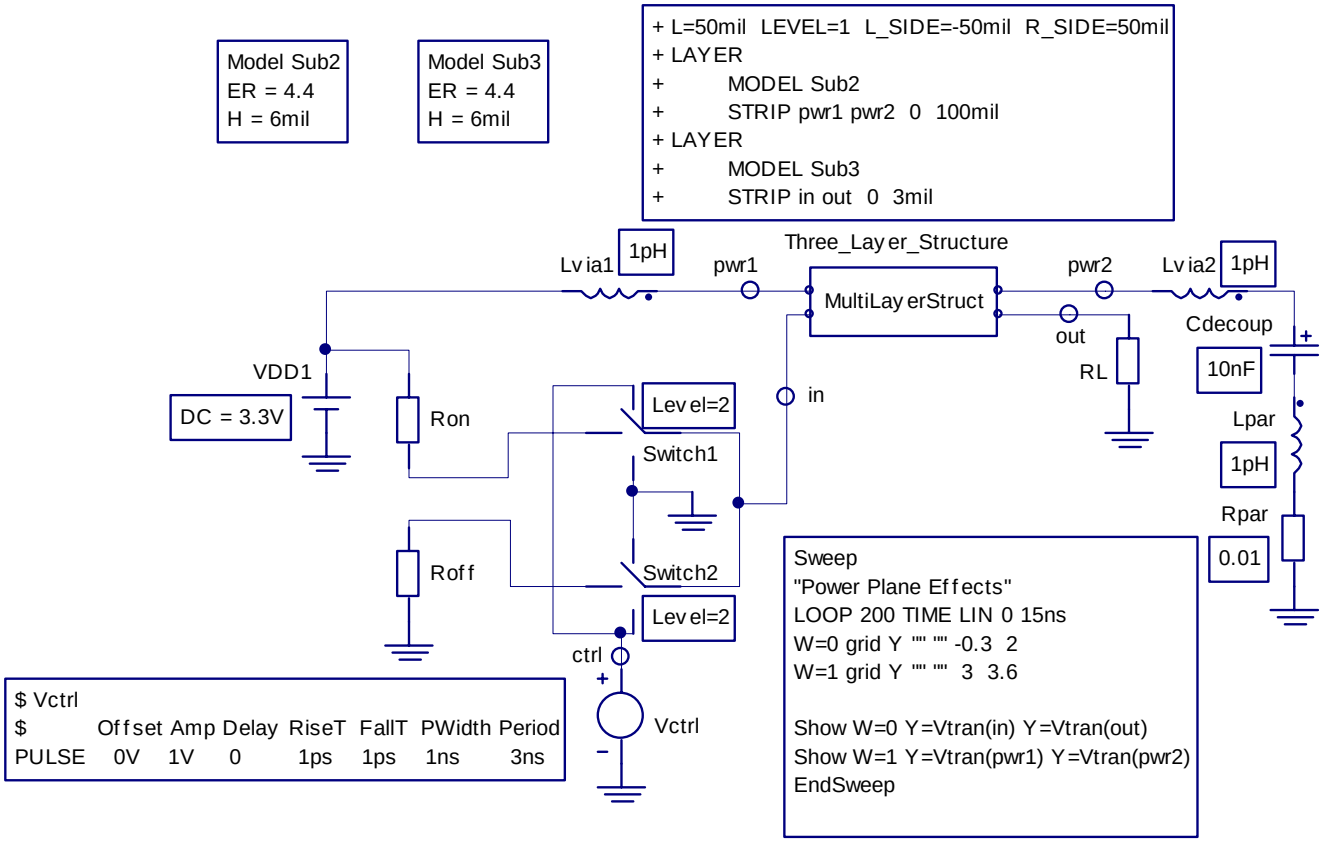


Using $R_{on} = R_{off} = R_L = Z_o$ as in the step b) above, you should obtain the following waveforms. Notice that now there is some deterioration of the signal integrity in both the input and output of the signal trace, and that there is severe interference in the power plane due to the signals in the return path.

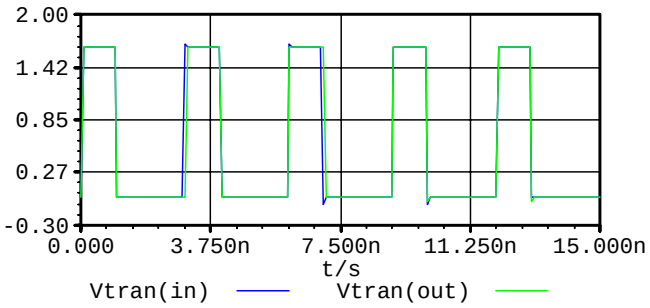


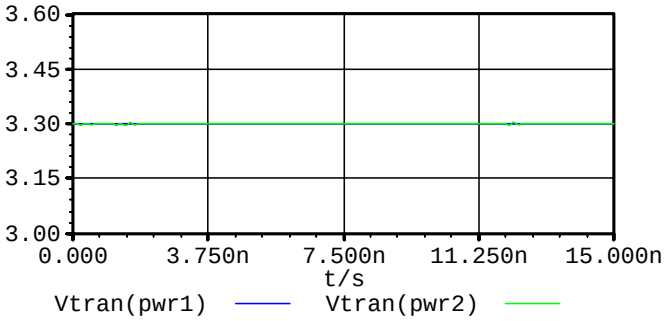


d) To alleviate the previous problem, you will connect a decoupling capacitor to the power plane through a via, as indicated in the following schematic. The decoupling capacitor will be modeled as an ideal capacitor of 10nF in series with a parasitic inductor of 1pH and a parasitic resistor of 10mΩ, as shown below.



Simulating the previous circuit in APLAC (using $R_{on} = R_{off} = R_L = Z_o$), you should get the following waveforms:





Notice that the signal integrity problems in both the signal path and the power plane have been eliminated by matching the source and the load to the stripline and by using the proper decoupling capacitor.

Submission deadline: Thursday May 18, 2006