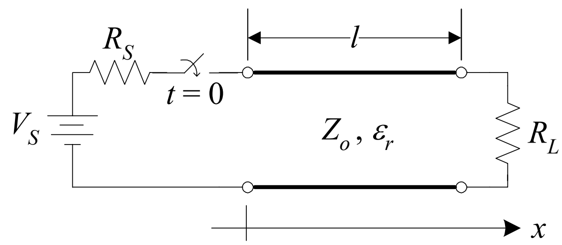
Signal Integrity and High-Speed Interconnects
Assignment 3

April 2006

Dr. J. E. Rayas Sánchez

Problem 1

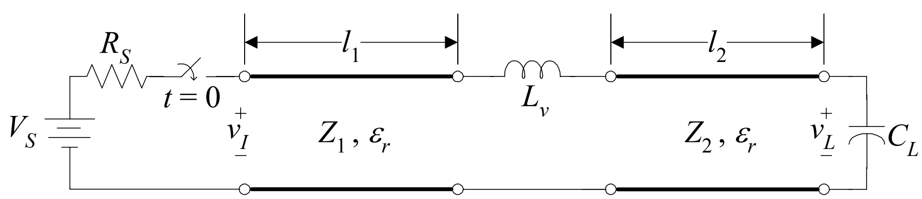
The circuit shown below has the following parameter values: V_S = 1.5V, R_S = 10 Ω, R_L = 100 Ω, Z_o = 50 Ω, ε_e = 3.35, and l = 16.39 cm.



Using a lattice diagram, plot the voltage at the input of the line, $v(x = 0, t)$, at the load, $v(x = l, t)$, and at the middle of the line, $v(x = l/2, t)$, from 0 to 6 ns. Verify your results by simulating the circuit in APLAC.

Problem 2

In this problem you will investigate the transient effects of inductive discontinuities in transmission line circuits with capacitive loads. The following circuit is a first-order model of two microstrip lines connected through a via. Each microstrip line is modeled with a lossless transmission line, and the via is modeled with a pure inductance L_v. The following parameter values are used: V_S = 3V, R_S = 25 Ω, C_L = 3 pF, $Z_1 = Z_2$ = 50 Ω, ε_e = 3, $l_1 = l_2$ = 8.6605 cm.

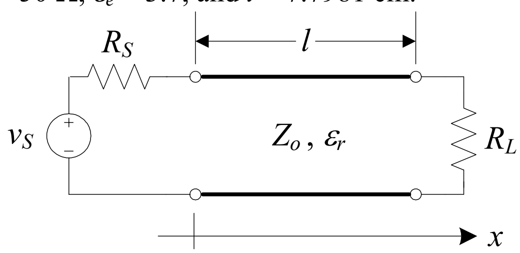


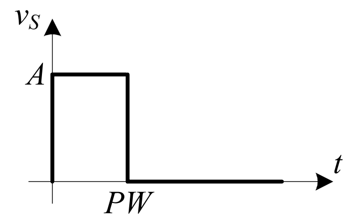
a) Simulate the circuit in APLAC using L_v = 0 H. Plot V_S, $v_I(t)$, and $v_L(t)$ from 0 to 10 ns. Verify that $v_I(0 < t < 2t_d) = V_o^+$ and that $v_I(2t_d) = -\Gamma_S V_o^+$, where t_d is the total flight time (or time delay) from the source to the load, and V_o^+ is the initial incident voltage wave amplitude at the input of the line.

b) Simulate the circuit in APLAC using L_v = 10 nH. Plot V_S, $v_I(t)$, and $v_L(t)$ from 0 to 10 ns. Verify that $v_I(0 < t < t_d) = V_o^+$ and that $v_I(2t_d) \neq -\Gamma_S V_o^+$. Notice that there is a new transient effect on v_I at $t = t_d$ due to the inductive discontinuity. Derive an expression to calculate $v_I(t_d)$.

Problem 3

The circuit shown below has the following parameter values: $A = 2$ V, $PW = 2$ ns, $R_S = 30\ \Omega$, $R_L = 80\ \Omega$, $Z_o = 50\ \Omega$, $\varepsilon_e = 3.7$, and $l = 7.7981$ cm.





Using a lattice diagram, plot the current at the input of the line, $i(x = 0, t)$, and at the load, $i(x = l, t)$, from 0 to 8 ns. Verify your results by simulating the circuit in APLAC.

Problem 4

Solve the problem 1 described above using Bergeron Diagrams.

Submission deadline: Thursday May 4, 2006