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Distortion Minimization for Packaging Level Interconnects

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Abstract

We propose a novel high-speed serial signaling scheme that minimizes the distortion for multichip module (MCM) packaging level communication by intentionally adding leakage resistors between the signal trace and the ground. The new scheme is inspired by the theory of distortionless transmission line which states that if R/G=L/C, there will be no distortion at the receiver end and the signal propagates at the speed of light. The simulation results indicate that, using the shunt resistor scheme, 10+ Gbps bit rate is achievable over a 10 cm single-ended stripline without pre-emphasis or equalization.

1. Introduction

With the ever increasing of device switching speed, system level interconnect performance has become a computing bottleneck. Recently, it has been demonstrated that sufficient bandwidth in the order of tens of Giga bit per second can be realized using simple resistive termination for on-chip interconnects [1] [2] [3] [4] [5]. Thus, we consider it an interesting question that how can we improve the capacity of packaging, PCB or even backplane level interconnects to fully utilize this abundant silicon computing power.

At packaging and PCB level, serial link performance is greatly restricted by signal distortion that creates inter-symbol interference (ISI). The fundamental reason for signal distortion over a serial channel is the frequency dependency of attenuation and phase velocity. Depending on the line property (cross-section geometry, length, resistivity, etc) and frequency of interest, interconnect at different scale could operate in one or more of the RC region, LC region and skin effect region [6]. For on-chip global interconnect, the series resistance is usually at the order of 10 Ω/mm and the skin effect is not significant. Thus on-chip interconnect primarily works in the RC region, or possibly in the LC region if the bit rate is high. By using a single resistive termination to crop the slow, less attenuated low frequency content, the distortion for on-chip global lossy line can be largely suppressed [5].

For packaging and PCB level interconnects, skin effect and proximity effect play an important role and the simple resistive termination scheme becomes insufficient. Conventional solutions to minimize the distortion for packaging interconnects include pre-emphasis, equalization and low voltage differential signalling (LVDS) techniques. In this paper, we propose to extend the Surfliner scheme [7] to multichip module packaging interconnect to minimize the distortion and maximize the channel capacity. The Surfliner scheme is based on the theory of distortionless transmission line which states that if $R/G = L/C$ then both the attenuation and phase velocity become frequency independent. However, for typical MCM traces the variation of R/L could be large, thus exact distortionless transmission may not be achievable. Surfliner seeks to approximate the behavior of distortionless T-Line by evenly adding leakage resistors between the signal trace and ground. Our simulation results indicate that, using the Surfliner scheme, 10+ Gbps transmission is achievable for a 10 cm long MCM single-ended stripline without any pre-emphasis and equalization. We also discuss the optimal value and spacing of the shunt resistors when Surfliner is applied to MCM traces.

The main contribution of this paper to demonstrate the feasibility and superiority of the Surfliner scheme for MCM packaging level interconnect.

2. Theory of Distortionless Transmission Line

We first give a quick review of the theory of distortionless transmission line [7] [8] for self-completeness of the paper. Rather than lumped circuit theory, transmission line theory treats any homogeneous metal interconnect as the conglomerate of numerous infinitesimal RLGC segments, one of which is shown in Fig. 1, where R, L, G, C are per unit length series resistance, self loop inductance, shunt conductance and shunt capacitance, respectively.

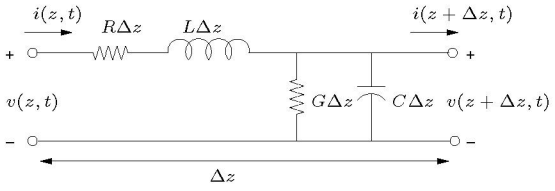

Fig. 1. RLGC model of a transmission line segment.

The voltage and current on the transmission line appear in the form of wave propagation; they are both functions of propagation distance z and time t, and are govern by the telegrapher's equations:

$$\frac{\partial V(z,t)}{\partial z} = -RI(z,t) - L\frac{\partial I(z,t)}{\partial t} \quad (1)$$

$$\frac{\partial I(z,t)}{\partial z} = -GV(z,t) - C\frac{\partial V(z,t)}{\partial t} \quad (2)$$

The general solution to the above telegrapher's equations can be expressed as:

$$V(z) = V^+(z) + V^-(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \quad (3)$$

where $V^+(z)$ and $V^-(z)$ are the waves travelling in $z+$ and $z-$ directions, respectively, and

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{4}$$

is the complex propagation constant. The real part of the propagation constant, α, is usually referred to as the *attenuation constant*, since 1 volt will attenuate to $e^{-\alpha}$ volt after travelling one unit distance. Similarly β is called the *phase constant*, because βz gives the phase of the voltage wave at location z. The velocity of the travelling wave is

$$v = \frac{\omega}{\beta} \tag{5}$$

The characteristic impedance of the line is defined as the ratio of voltage to current at any point of the line:

$$Z_0 = \frac{V^+(z)}{I^+(z)} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{6}$$

From Eqn. (4) we see that both α and ω/β are functions of the frequency. Depending on the RLGC values and frequency, the transmission line can operate in the RC region, LC region or skin effect region, and each performance region has its unique properties [6]. Nevertheless, in general high-frequency components tend to travel faster, but attenuate more comparing to the low-frequency components. When an ideal digital pulse train is transmitted over the channel, this frequency dependency of attenuation and phase velocity will result in distortion[1] of the waveform, causing inter-symbol interference (ISI).

Interestingly if we set

$$\frac{R}{G} = \frac{L}{C} \tag{7}$$

and substitute the relation into Eqn. (4) and (6), we have

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(RC/L + j\omega C)} = \frac{R}{\sqrt{L/C}} + j\omega\sqrt{LC} \tag{8}$$

$$Z_0 = \sqrt{\frac{L}{C}} \tag{9}$$

Therefore, $\alpha = R/\sqrt{L/C} = R/Z_0$ and $v = \omega/\beta = 1/\sqrt{LC} = c_0/\sqrt{\epsilon_r}$. Assuming RLGC themselves are constant, we now obtain frequency-independent attenuation and phase velocity across the whole spectrum. And the phase velocity is actually the speed of light in the dielectric. The characteristic impedance (Eqn. (9)) becomes pure resistive.

Eqn. (7) is usually referred to as Heaviside condition to credit Oliver Heaviside who first discovered this elegant result [9]. Based on this result Heaviside proposed to deliberately add inductance for transatlantic cable to achieve distortionless communication, and that was one hundred years ago! For MCM application, inductance is hard to control, instead we could evenly insert leakage resistors to approximate the Heaviside condition.

3. Case Study

In this section, we use a real design case to illustrate the feasibility and superiority of the Surfliner scheme using shunt resistors. To get a better demonstration we use a single-ended stripline instead of a differential pair. The cross section of the MCM stripline is shown in Fig. 2. The geometry of the cross section is based on the data for IBM high-end AS/400 systems [10] except that, to minimize the impact of skin effect, we set the thickness of the signal line to be 2 μm, which is the minimum metal thickness that can be processed by state-of-the-art MCM packaging stack up technology. We assume the resistivity of pure copper, ρ=1.72e-06 S/cm. For the insulator we assume liquid crystal polymer (LCP) which has a small dissipation factor of 0.0025 yet is much cheaper than ceramics [11]. The line length is 10 cm.

3.1. Optimal Shunt Conductance

The first step in designing the distortionless T-Line is to determine the shunt conductance. In Eqn. (7), a hidden assumption is that RLC values of the T-Line is independent of the frequency so that we can find a single G to meet the Heaviside condition. However, this is not the real scenario. For MCM traces, the resistance and inductance values change significantly over frequency due to skin effect and proximity effect. Thus a single conductance value for meeting the Heaviside condition at all frequency points is not possible. This brings up the question of what is the optimal shunt conductance.

We use a 2D EM solver called CZ2D from IBM to extract the RLGC values of the MCM stripline up to 50 GHz, and the results are shown in Fig. 4. CZ2D is part of the IBM electromagnetic field solver suite. It has the capability to consider both skin-effect and proximity effect yet it is much faster than 3D extraction tools such as Raphael [12]. Clearly, as the frequency passes roughly 1 GHz, the line resistance starts to increase first due to the proximity effect to the ground, and then due to the skin effect. Meanwhile, the total inductance decreases because the internal inductance of the line vanishes when currents rush to the surface of the conductor. The capacitance, on the other hand, is virtually constant over the whole spectrum. The leakage conductance due to the dielectric, though increases sharply at high frequencies, is still negligible comparing to the series line resistance. The high-frequency characteristic impedance of the line is Z_0=78 Ω. Note that the characteristic impedance of typical PCB traces is 50 Ω, thus if the MCM trace goes off to the board there will be impedance mismatch. However, if the MCM trace stays on the packaging we would rather have a larger Z_0 because that will minimize the attenuation. The line delay is 57.78 ps/cm.

As we have discussed in Section 2, at high frequencies the T-Line operates in the good LC region or skin effect region. It is in the RC region that both attenuation and phase velocity see great frequency dependency. Therefore, our rule of thumb for determining shunt

[1]More precisely, the spreading of the waveform due to phase velocity difference is termed dispersion.

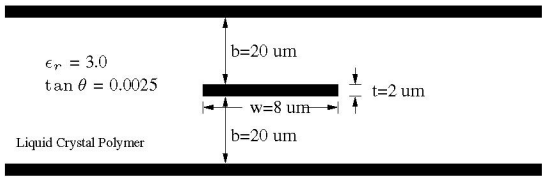

Fig. 2. Cross section of the 10 cm MCM stripline trace.

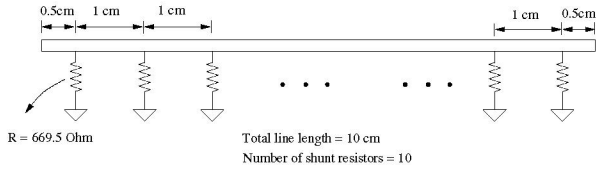

Fig. 3. Schematic of the Surfliner scheme using evenly spaced shunt resistors.

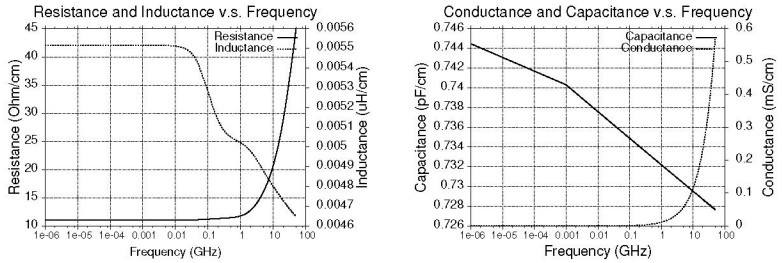

Fig. 4. RLGC values v.s. frequency for the 10 cm MCM stripline

conductance is "match-at-DC". Near DC mode, we have $R_{1\text{MHz}}$=11.07 Ω/cm, $C_{1\text{MHz}}$=0.74 pF/cm and $L_{1\text{MHz}}$=5.52e-03 μH/cm. The total shunt resistance needed for meeting the Heaviside condition for the 10 cm stripline is

$$R_{\text{shunt,total}} = \frac{L_{1\text{MHz}} \cdot 10cm}{(R_{1\text{MHz}} \cdot 10cm)(C_{1\text{MHz}} \cdot 10cm)} = 66.95\ \Omega \tag{10}$$

3.2. Simulation Results

Assuming we evenly insert N shunt resistors for the 10 cm line, each resistor has the value

$$R_{\text{single}} = N \cdot R_{\text{shunt,total}} \tag{11}$$

In theory, we can increase N so that the line approaches a distributive distortionless T-Line. However, inserting too many shunt resistors can be prohibitive in terms of resources, nor is it necessary. According to our simulation, if the spacing of the shunt resistors is less than the critical length $l_{\text{crit}} = \frac{c}{\sqrt{\epsilon_r}} \cdot T_{\text{cycle}}$, where T_{cycle} is the cycle time of the signal, the transient response of the system becomes very close to that of a real distributive distortionless T-Line. If the system is targeted for 10 Gbps data transmission, the critical length l_{crit} is roughly 1.7 cm. Thus, for our 10 cm stripline we insert a shunt resistor of 669.5Ω every 1 cm. The resistors can be implemented using embedded carbon film paste which has flexible sheet resistance depending on the amount of carbon in it. The design is shown in Fig. 3.

Fig. 5 shows the pulse responses of the 10 cm line w/o shunts and with 10 shunt resistors inserted. The input is a trapezoidal pulse with 10 ps rising/falling time and 170 ps duration. For the raw RLGC T-Line without shunts, we see both slow rising top, long tail and reflections which will lead to significant ISI. For the T-Line with 10 shunts, the pulse shape is largely preserved, but the height is reduced to approximately 0.5 volt. The DC saturation voltage, in this case, is determined by the resistance ladder formed by the series line resistance and shunt resistors. At the receiver side, a state-of-the-art sense amplifier can easily detect this amount of voltage. Both responses rise at about 600 ps, which corresponds to the time of flight of the 10 cm line.

The advantage of the shunted T-Line can also be explained in terms of the attenuation and phase velocity. Fig. 8 shows $e^{-\alpha}$ and phase velocity for both shunted T-Line and raw RLGC T-Line. We see that for shunted T-Line, the variation of attenuation over frequency is less severe than that of raw RLGC T-Line, although the overall curve is lower. More importantly, for shunted T-Line the velocity of the low-frequency components is greatly boosted up and the phase velocity curve is flat. In the case of raw RLGC T-Line, the signal speed goes up from almost zero at DC and saturates at the speed of light when the frequency increases.

The performance of the shunted T-Line in Fig. 3 is evaluated by Hspice simulation. Each 0.5cm/1cm wire segment is modelled using W-element with the frequency dependent RLGC tabular model, which is extracted using CZ2D. The input is 1000 bit pieces of a 10 Gbps pseudo random bit sequence (PRBS). The rising/falling edges are set to be 10% of the cycle time. The eye diagram at the receiver side, as shown in Fig. 6, presents a very clear opening. The maximum eye opening voltage is 0.43 volt with 0.5 volt DC saturation voltage, and the jitter is only 5.4 ps. On the other hand, the eye diagram of the raw RLGC line in Fig. 7 shows much worse timing/noise margin. The maximum eye opening is 0.51 volt out of 1 volt DC saturation voltage, and the jitter is 22.5 ps.

To study the effect of RL variation, we change the thickness of the signal line to 4.5 μm and conduct the same design procedures as described above. The resulted eye diagrams for the raw RLGC line and shunted line are shown in Fig. 9 and Fig. 10, respectively. In both cases, the eye diagram is inferior to that of the 2 μm thick line because of larger RL variation. Nevertheless, the benefit of adding shunt resistors is clear.

4. Conclusion

By introducing leakage resistors to meet the Heaviside condition, near distortionless signaling for MCM packaging level interconnect with speed of light is achievable. In principle, this shunt resistor scheme can also be applied to PCB dimension traces. For future work we would like to fully exploit the potential of this new scheme for differential signaling or other wire configurations, and consider its application in system level design.

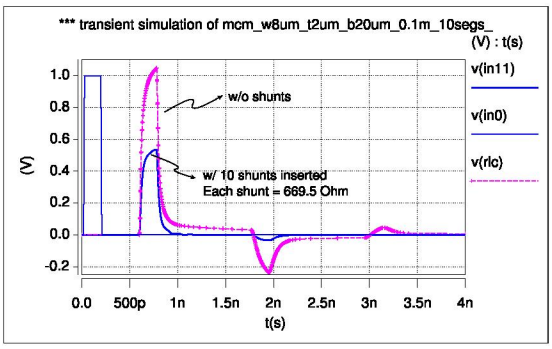

Fig. 5. Pulse responses of the w8μm/t2μm/b20μm/L10cm MCM stripline with and without shunt resistors.

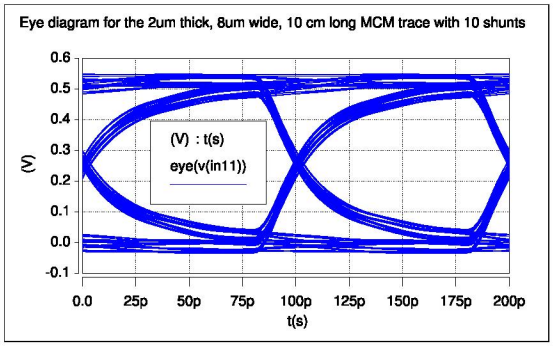

Fig. 6. Eye diagram for the w8μm/t2μm/b20μm/L10cm MCM stripline with 10 shunt resistors inserted (each shunt resistor = 669.5Ω).

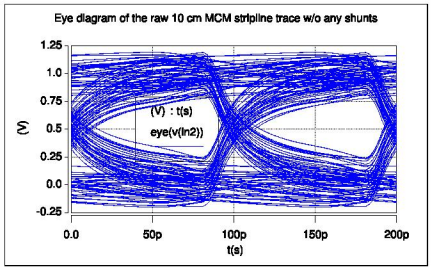

Fig. 7. Eye diagram for the w8μm/t2μm/b20μm/ L10cm MCM stripline w/o shunts.

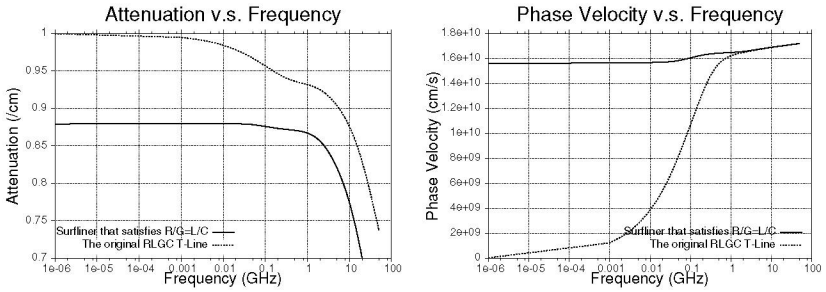

Fig. 8. Attenuation and phase velocity v.s. frequency for the 10 cm MCM stripline.

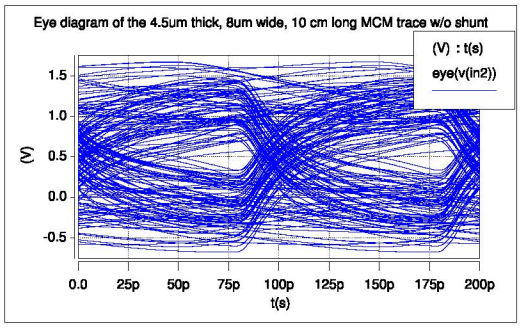

Fig. 9. Eye diagram for the w8μm/t4.5μm/b20μm/L10cm MCM stripline.

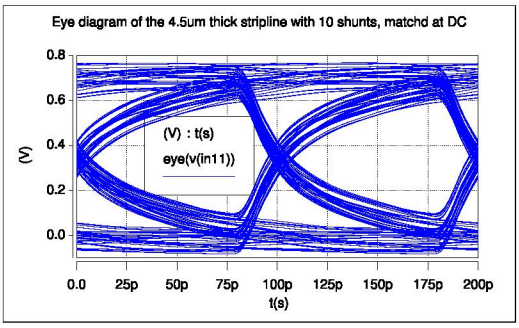

Fig. 10. Eye diagram for the w8μm/t4.5μm/b20μm/L10cm MCM stripline with 10 shunt resistors.

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