Electronics II
(02 SE048)

Lab Experiment 1 (option B):
MOSFET Differential Amplifiers

Objectives

The general objective of this experiment is to contrast the practical behaviour of a real differential pair with its theoretical version. Other more specific objectives are:

a) to reinforce practical techniques to measure the most important MOSFET internal parameters

b) to verify the differential and common mode operation

c) to design a MOSFET differential amplifier.

Components and Instrumentation

1 CD4007 (CMOS transistor array, see the appendix)

Several resistors (1% tolerance if possible, to facilitate matching the differential pairs)

Two variable DC power supplies (0 to 20 V)

A waveform generator

A DMM with 2½ or more digits and resistance measurement capability

A two-channel oscilloscope with x10 or x1 probes

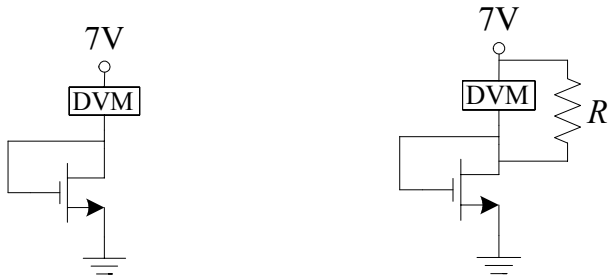
Theoretical Procedure, Part A

A simple and effective method for measuring V_{th} and K for an n-channel MOSFET is illustrated in Fig. 1. From Fig. 1a, explain how V_{th} can be calculated by reading the DVM voltage. Once V_{th} is known, explain how K can be calculated by reading the DVM voltage for the circuit in Fig. 1b.

A similar procedure can be used for p-channel MOSFETs. Fig. 2 shows the corresponding circuits. Explain the procedures to measure V_{th} and K for a P-MOSFET.

Lab Procedure, Part A

As seen in the appendix, the CD4007 CMOS array consists of 6 transistors, 3 p-channel and 3 n-channel, interconnected to some extent in order to reduce the number of IC pins required. One critical issue is that pins 14 and 7 are the substrate connections for all the p-channel and all the n-channel devices,



(a) (b)

Fig. 1 A simple technique to measure the internal parameters of a n-channel MOSFET: (a) measuring V_{th}, (b) measuring K.

respectively. P-channel substrate (pin 14) must be connected to the most positive voltage supply in use, while the n-channel substrate (pin 7) must be connected to the most negative voltage supply in use. These connections must be done no matter what use is made of any device. Also notice from the appendix that the maximum voltage allowed between pin 14 and pin 7 is 18V, otherwise internal voltage breakdown may result.

Assemble the circuit shown in Fig. 1a for each of the three n-channel MOSFETs, and measure V_{th} for each of them.

Using a resistor R of a suitable value, assemble the circuit shown in Fig. 1b for each of the three n-channel MOSFETs, and measure K for each of them.

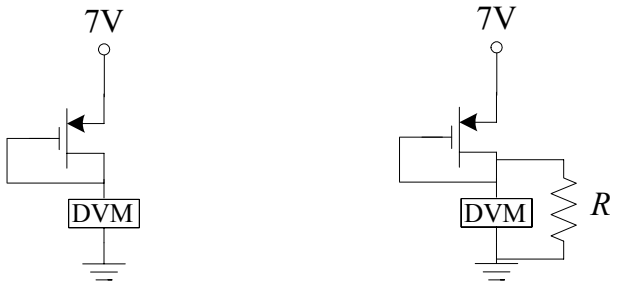
Assemble the circuit shown in Fig. 2a for each of the three p-channel MOSFETs, and measure V_{th} for each of them.

Using a resistor R of a suitable value, assemble the circuit shown in Fig. 2b for each of the three p-channel MOSFETs, and measure K for each of them.

Create a table to display V_{th} and K for each of the six MOSFETs, and indicate the value of R used. Label this table as "Table I".

Theoretical Procedure, Part B

Design a differential amplifier biased with a simple resistor using two of the n-channel MOSFETs available in a single CD4007. Use the internal parameter values previously measured for the transistors. Calculate the resistor values and the voltage supply values such that the DC operating current, I_{DSQ}, is 1 mA and the magnitude of the differential mode voltage gain, $|A_d|$, is 5. Calculate all the DC voltages and currents in the circuit.



(a) (b)

Fig. 2 A simple technique to measure the internal parameters of a p-channel MOSFET: (a) measuring V_{th}, (b) measuring K.

Lab Procedure, Part B

Implement your differential amplifier designed. Use 1% tolerance resistors and make sure that they are as well-matched as you can make them (use your digital ohmmeter if necessary). Measure the DC voltages on all the nodes and calculate from them all currents in the circuit. Create a table to display all the DC values measured and the corresponding theoretical ones. Label this table as "Table II".

Measure the differential mode (single-ended) voltage gain and the common-mode voltage gain. As an input signal, use a generator to provide a sine wave of 1Vpp at 1KHz. Plot the corresponding waveforms as seen in the oscilloscope and create a table to compare your theoretical predictions with your lab measurements. Create a table to display all the voltage gains, measured and calculated. Label this table as "Table III".

Report

Write a report including all the theoretical and lab procedures as well as your conclusions. Make sure to include in your report the 3 tables described before. For tables II and III, indicate the percentage of error of the quantities measured with respect to those calculated theoretically.

Deadline and Assessment

The deadline for submitting the report is on Wednesday September 17, 2003. The report can be written in either English or Spanish.

This lab experiment can be realized in teams of up to 3 students. The evaluation of the report will be as follows:

Quality of the report	30%
Accuracy of the theoretical analysis	30%
Lab measurements and procedures	40%

If the report is written in acceptable English, an extra 10% can be granted.

TEXAS INSTRUMENTS

CD4007UB Types

CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

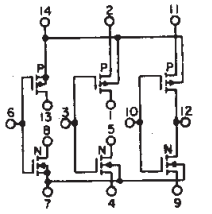
■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative **Standard No. 13B, "Standard Specifications** for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



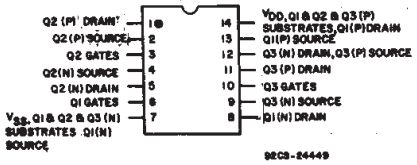
Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

FUNCTIONAL DIAGRAM

Applications:

- Extremely high-input impedance amplifiers
- Shapers
- Inverters
- Threshold detector
- Linear amplifiers
- Crystal oscillators

TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0;10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				—	—	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS	LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance	C_{IN}	Any Input	10	15	pF

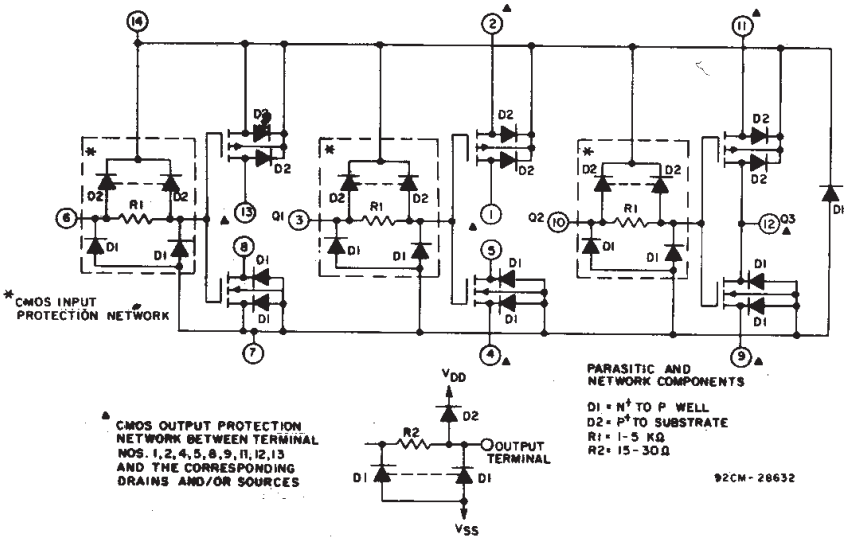
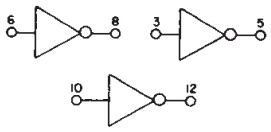


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

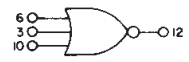
a) Triple Inverters



(14,2,11); (8,13); (1,5); (7,4,9)

92CS-15350

b) 3-Input NOR Gate



(13,2); (1,11); (12,5,8); (7,4,9)

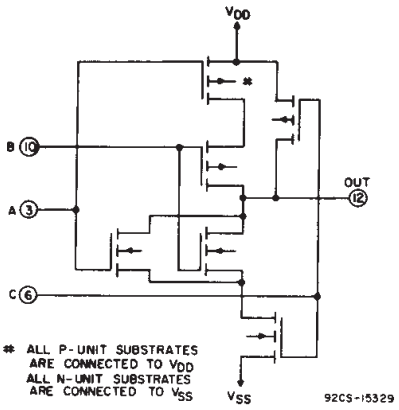
92CS-15349

c) 3-Input NAND Gate

(1,12,13); (2,14,11); (4,8); (5,9)

92CS-15348

d) Tree (Relay) Logic



(13,12,5); (4,9,8); (14,2); (1,11)

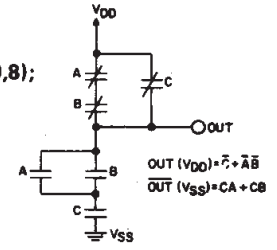
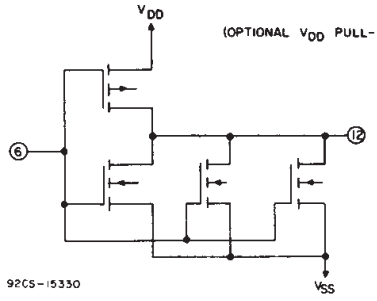


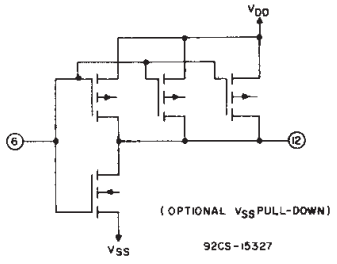
Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB.

e) High Sink-Current Driver

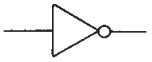


(6,3,10); (8.5, 12); (11,14); 7,4,9)

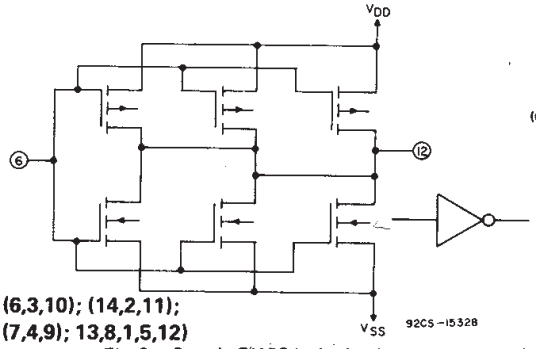
f) High Source-Current Driver



(6,3,10); (13,1,12); (14,2,11); (7,9)

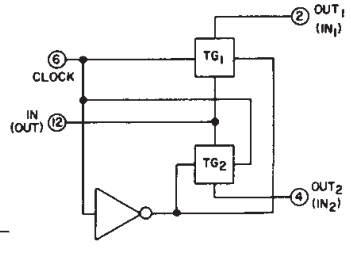


g) High Sink - and Source-Current Driver



(6,3,10); (14,2,11); (7,4,9); 13,8,1,5,12)

h) Dual Bi-Directional Transmission Gating



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB (Cont'd).

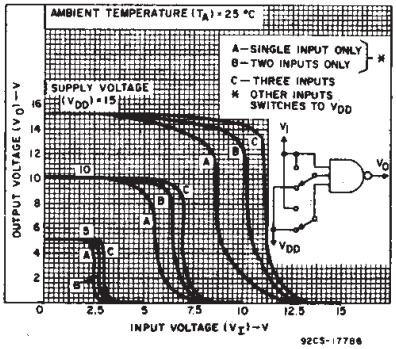


Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

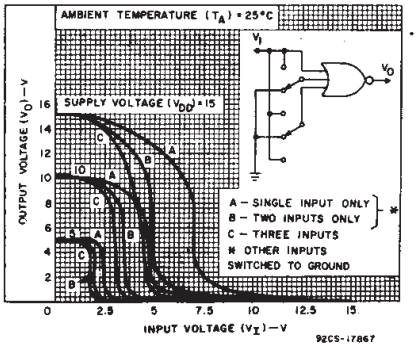


Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

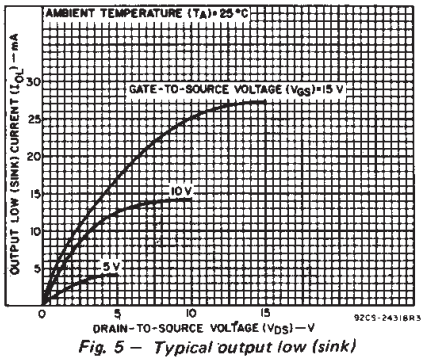


Fig. 5 – Typical output low (sink) current characteristics.

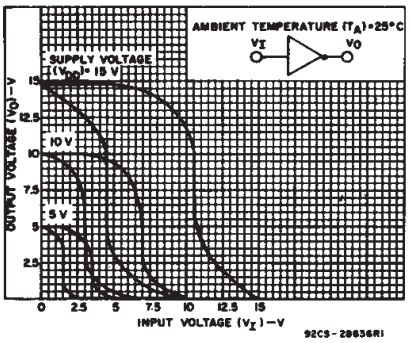


Fig. 6 – Minimum and maximum voltage-transfer characteristics for inverter.

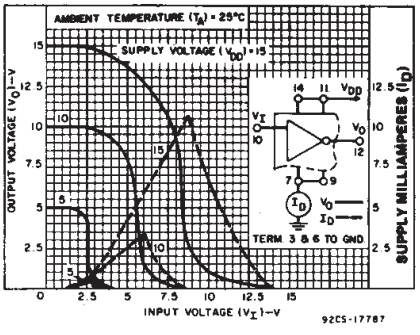


Fig. 7 – Typical current and voltage-transfer characteristics for inverter.

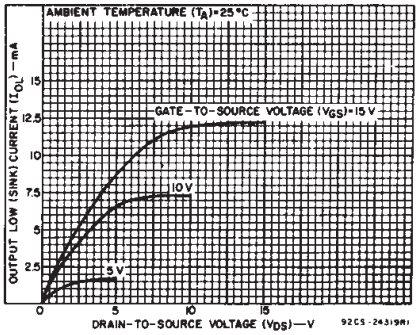


Fig. 8 – Minimum output low (sink) current characteristics.

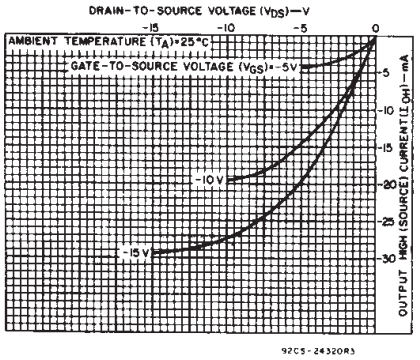


Fig. 9 – Typical output high (source) current characteristics.

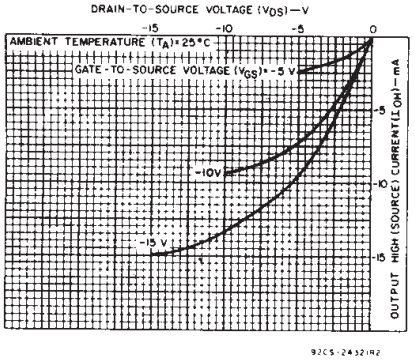


Fig. 10 – Minimum output high (source) current characteristics.

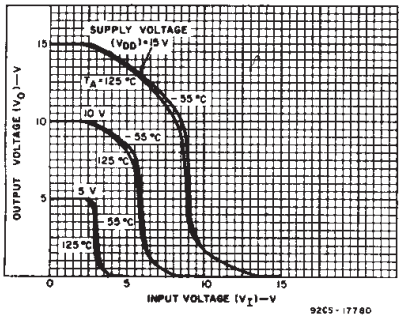


Fig. 11 – Typical voltage-transfer characteristics as a function of temperature.

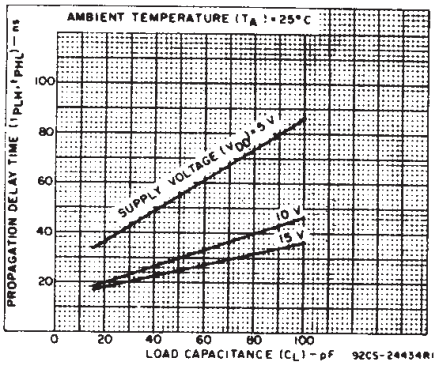


Fig. 12 – Typical propagation delay time vs. load capacitance.

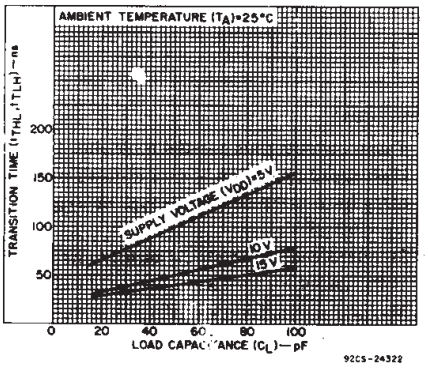


Fig. 13 – Typical transition time vs. load capacitance.

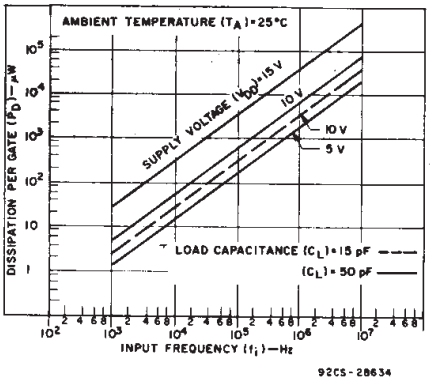


Fig. 14 – Typical dissipation vs. frequency characteristics.

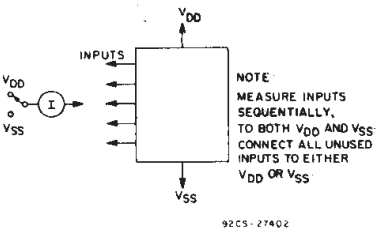


Fig. 15 – Input current test circuit.

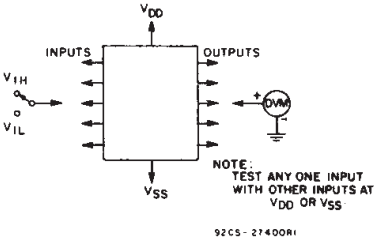


Fig. 16 – Input voltage test circuit.

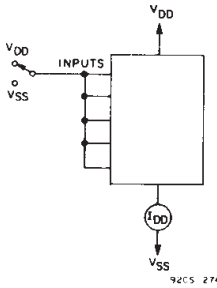
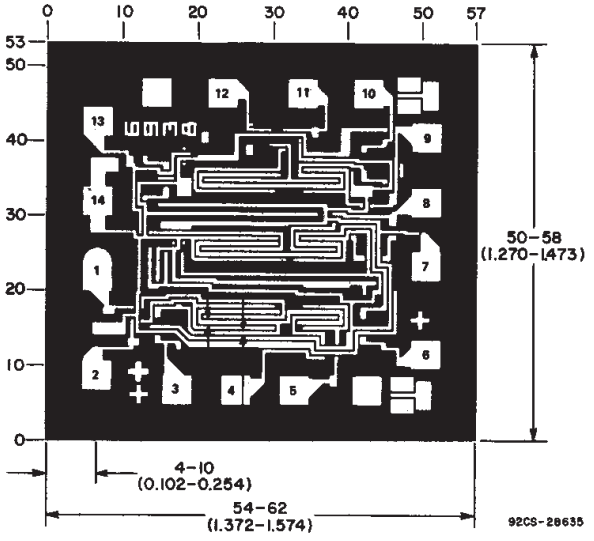


Fig. 17 – Quiescent device current test circuit.



DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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