Electronics II
(02 SE048)

Lab Experiment 1 (option A):
BJT Differential Amplifiers

Objectives

The general objective of this experiment is to contrast the practical behaviour of a real differential pair with its theoretical version. Other more specific objectives are:

a) to reinforce the notion of common-emitter half circuits in the process of design and analysis of a differential amplifier

b) to verify the differential and common mode operation

c) to design a current mirror and apply it to bias a differential pair.

Components and Instrumentation

1 CA3046, MC3346, LM3086 or LM3046 (BJT npn transistor array, see the appendix)

Several resistors (1% tolerance if possible, to facilitate matching the differential pairs)

1 potentiometer (around 1KΩ)

two variable DC power supplies (0 to 20 V)

a waveform generator

a DMM with 2½ or more digits and resistance measurement capability

a two-channel oscilloscope with x10 probes

Theoretical Procedure, Part A

Calculate all the DC voltages and currents in the two differential half-circuits shown in Fig. 1 (refer to the appendix for the internal parameters of the transistors).

Lab Procedure, Part A

Assemble the circuit of Fig. 1 using resistors that are as well-matched as you can make them (use your digital ohmmeter if necessary). Please note that in the 3046 array pin 13 must be connected to the most negative voltage supplied to any of the devices, since all the devices in this chip are fabricated on a common substrate.

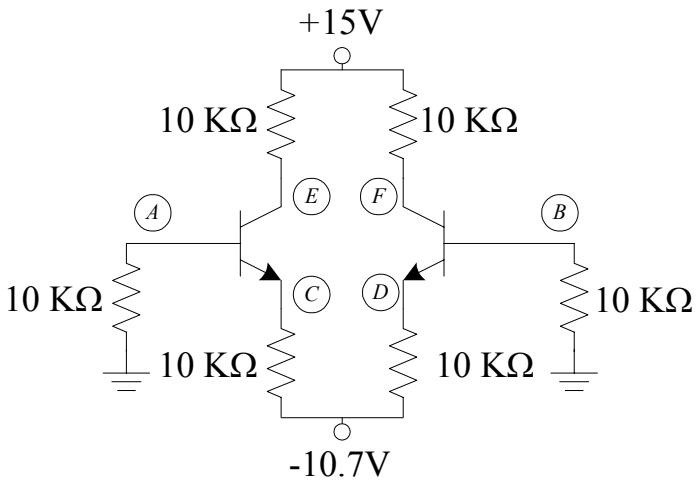


Fig. 1. Two differential half-circuits.

Measure the voltages at nodes *A* through *F*. From these measurements calculate the currents in all the branches as well as α_1, α_2, β_1 and β_2, as well as V_{BE1} and V_{BE2}.

Create a table to compare these results with your theoretical results previously calculated. Label this table as "Table I".

Join nodes *C* and *D* (which should have nearly the same voltage) and measure again the voltages on nodes *A* through *F*. Note that they are virtually the same as before.

With nodes *C* and *D* joined, *A* unchanged and *B* connected via a 1MΩ resistor to the center of a 1KΩ potentiometer, R_p, connected between +15V and –10.7V, measure the voltage between nodes *E* and *F*. Adjust R_p until this is exactly zero. Measure the voltages at *A* through *F* and *P* (the center of R_p). You have in effect compensated for the total input offset including the voltage offset resulting from base-emitter mismatch, and the difference in bias-current flow (i.e., offset current) in the base resistors R_B. What is the total input offset voltage and the average offset current?

Create a table to display the voltages on nodes *A* through *F* before and after the compensation procedure. Label this table as "Table II".

Theoretical Procedure, Part B

Calculate the voltage gain from *A* to *E* (v_e/v_a) for the circuit shown in Fig. 2 (refer to the appendix for the internal parameters of the transistors). Calculate the input impedance at node *A*. Calculate the voltage gain from *A* to *E* (v_e/v_a) when node *B* is not grounded and connected to node *A* (common-mode operation).

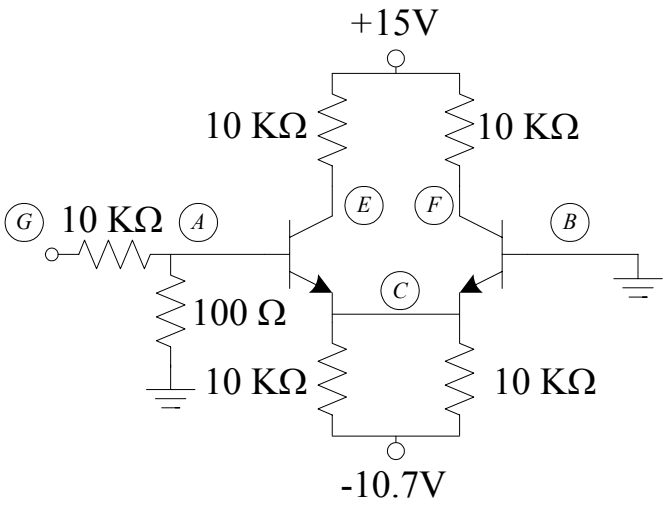


Fig. 2. Simple differential amplifier.

Lab Procedure, Part B

Assemble the circuit of Fig. 2. Connect a generator to provide a sine wave of 1Vpp at 1KHz at node *G*. Using a two-channel oscilloscope, measure the voltage gain from *A* to *E* (v_e/v_a). Plot v_a, v_e and v_f as they appear in the oscilloscope. Why was the voltage divider of 10KΩ-100Ω added to the circuit?

Measure the input impedance at node *A* (after the 100Ω resistor). Describe the method used to measure this impedance.

Measure the voltage gain from *A* to *E* (v_e/v_a) when node *B* is not grounded and connected to node *A* (common-mode operation). Plot v_a, v_e and v_f as they appear in the oscilloscope.

Create a table to compare this results with your theoretical results previously calculated (voltage gains and input impedance). Label this table as "Table III".

Theoretical Procedure, Part C

Design a differential amplifier biased with a current mirror (any configuration) using the transistors available in a single chip 3046. Calculate all the DC voltages and currents in the circuit. Calculate the differential mode (single-ended) voltage gain and the common-mode voltage gain. Refer to the appendix for the internal parameters of the transistors.

Lab Procedure, Part C

Implement your designed differential amplifier biased with a current mirror. Measure the DC voltages on all the nodes and calculate from them all currents in the circuit. Measure the differential mode (single-ended) voltage gain and the common-mode voltage gain. Plot the corresponding waveforms as seen in the oscilloscope and create a table to compare your theoretical predictions with your lab measurements. Label this table as "Table IV".

Report

Write a report including all the theoretical and lab procedures as well as your conclusions. Make sure to include in your report the 4 tables described before. For each table, indicate the percentage of error of the quantities measured with respect to those calculated theoretically.

Deadline and Assessment

The deadline for submitting the report is on Wednesday September 17, 2003. The report can be written in either English or Spanish.

This lab experiment can be realized in teams of up to 3 students. The evaluation of the report will be as follows:

Quality of the report	30%
Accuracy of the theoretical analysis	30%
Lab measurements and procedures	40%

If the report is written in acceptable English, an extra 10% can be granted.

National Semiconductor

July 1999

LM3046
Transistor Array

General Description

The LM3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3046 is supplied in a 14-lead molded small outline package.

Features

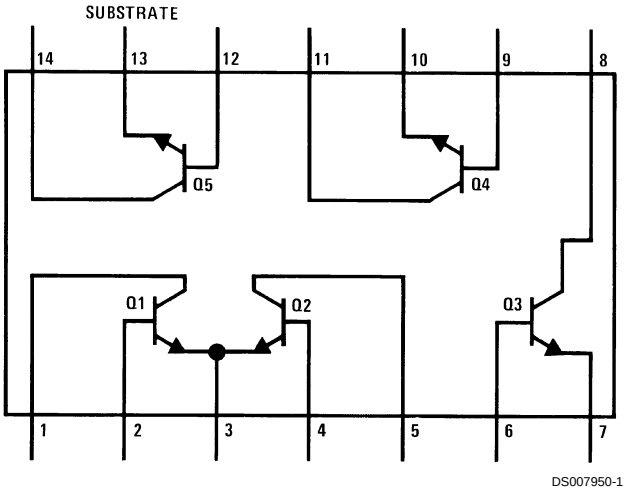
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 µA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure: 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Small Outline Package



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Top View
Order Number LM3046M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (T_A = 25˚C)

	LM3046		
	Each Transistor	**Total Package**	**Units**
Power Dissipation:			
T_A = 25˚C	300	750	mW
T_A = 25˚C to 55˚C	300	750	mW
T_A > 55˚C	Derate at 6.67		mW/˚C
T_A = 25˚C to 75˚C			mW
T_A > 75˚C			mW/˚C
Collector to Emitter Voltage, V_{CEO}	15		V
Collector to Base Voltage, V_{CBO}	20		V
Collector to Substrate Voltage, V_{CIO} (Note 2)	20		V
Emitter to Base Voltage, V_{EBO}	5		V
Collector Current, I_C	50		mA
Operating Temperature Range	−40˚C to +85˚C		
Storage Temperature Range	−65˚C to +85˚C		
Soldering Information			
Dual-In-Line Package Soldering (10 Sec.)	260˚C		
Small Outline Package			
Vapor Phase (60 Seconds)	215˚C		
Infrared (15 Seconds)	220˚C		

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics

(T_A = 25˚C unless otherwise specified)

Parameter	Conditions	Limits			Units
		Min	**Typ**	**Max**	
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10 µA, I_E = 0	20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10 µA, I_{CI} = 0	20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E 10 µA, I_C = 0	5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0.002	40	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			0.5	µA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V, I_C = 10 mA		100		
	I_C = 1 mA	40	100		
	I_C = 10 µA		54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{IO2}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.3	2	µA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1 mA		0.715		V
	I_E = 10 mA		0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4}\rvert$, $\lvert V_{BE4} - V_{BE5}\rvert$, $\lvert V_{BE5} - V_{BE3}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5	mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		−1.9		mV/˚C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		0.23		V

Electrical Characteristics (Continued)

(T_A = 25˚C unless otherwise specified)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		1.1		µV/˚C

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

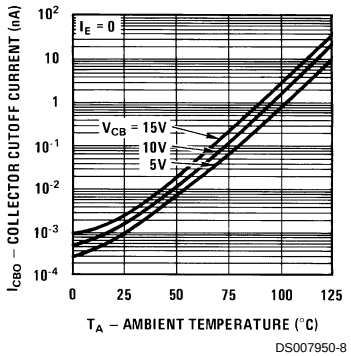
Note 2: The collector of each transistor is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 µA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		µmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3+J 0.04		
Output Admittance (Y_{oe})			0.001+j 0.03		
Reverse Transfer Admittance (Y_{re})			See Curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



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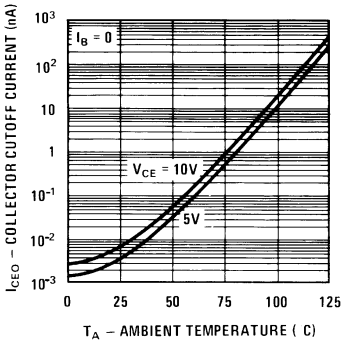
Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor



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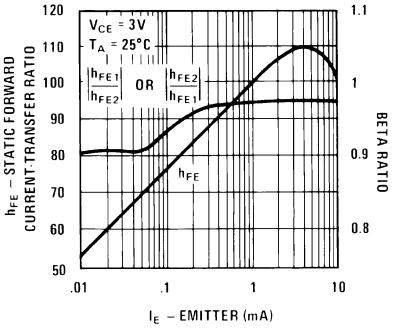
Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current



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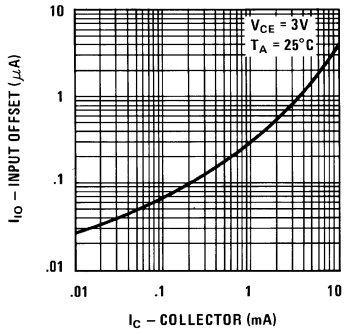
Typical Performance Characteristics (Continued)

Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current



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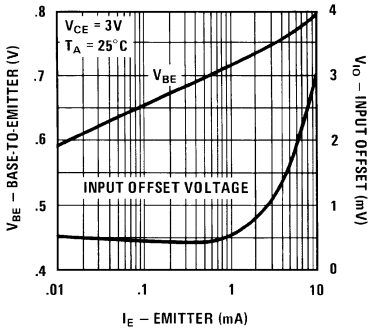
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



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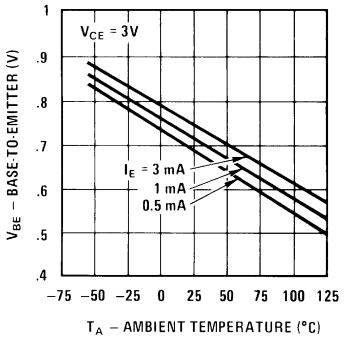
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



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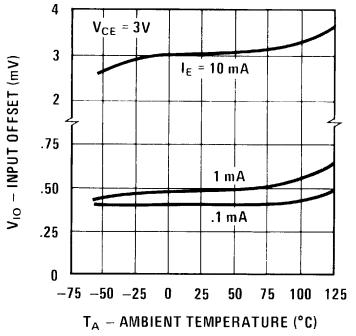
Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature



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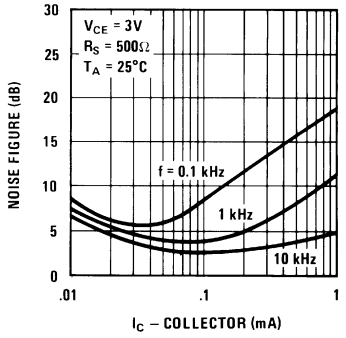
Typical Noise Figure vs Collector Current



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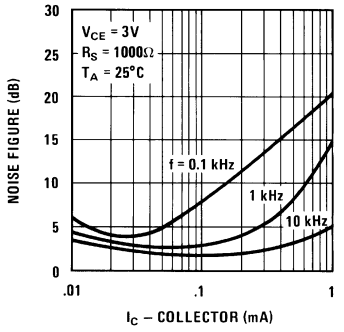
Typical Noise Figure vs Collector Current



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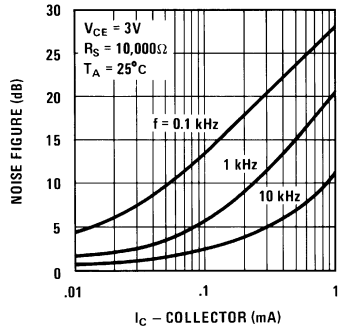
Typical Noise Figure vs Collector Current



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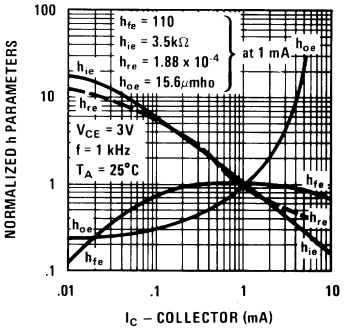
Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



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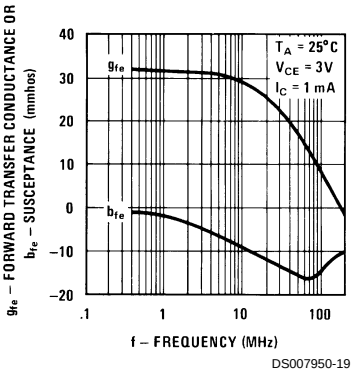
Typical Forward Transfer Admittance vs Frequency



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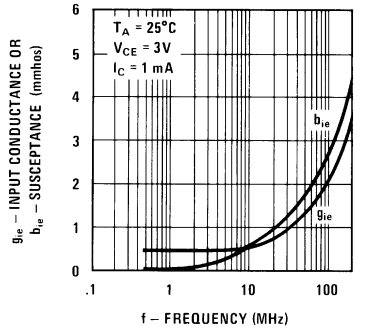
Typical Performance Characteristics (Continued)

Typical Input Admittance vs Frequency



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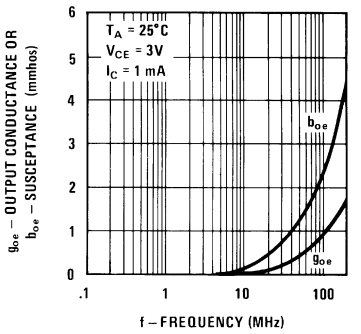
Typical Output Admittance vs Frequency



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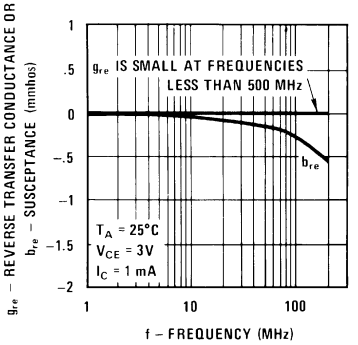
Typical Reverse Transfer Admittance vs Frequency



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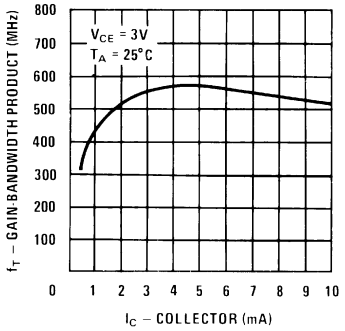
Typical Gain-Bandwidth Product vs Collector Current



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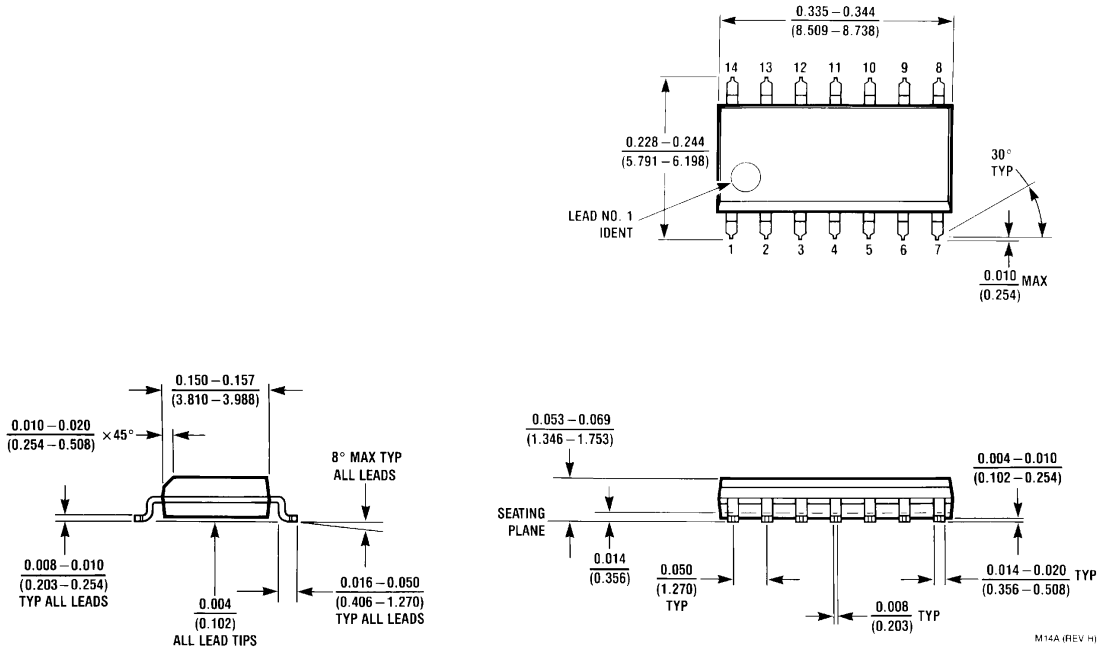
Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M)
Order Number LM3046M
NS Package Number M14A

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