FET Small-Signal Models

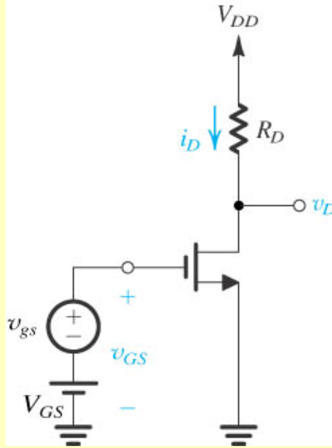
Dr. José Ernesto Rayas Sánchez

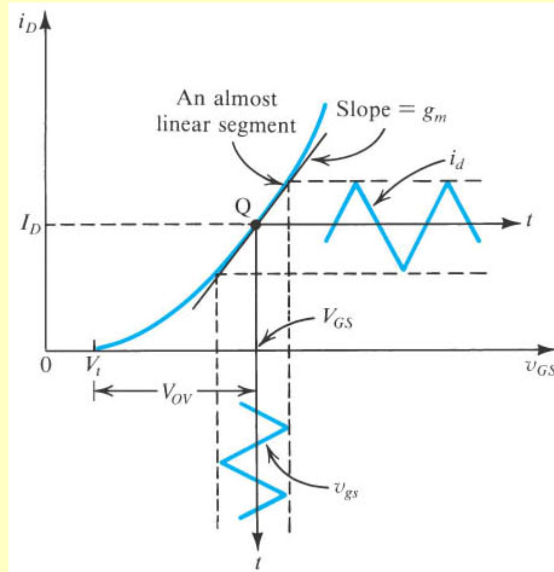
Some figures of this presentation were taken from the instructional resources of the following textbook:
A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. New York, NY: Oxford University Press, 2003.

Outline

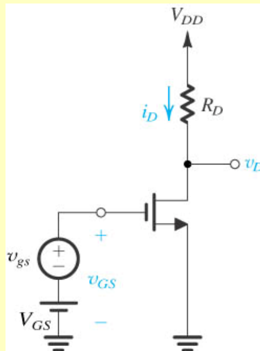
- DC Bias + small-signal excitation
- Load lines
- Amplification process in FETs
- Small-signal models
- DC and small-signal analysis: example
- Manufacturing data sheets

DC Bias + Small-Signal Excitation



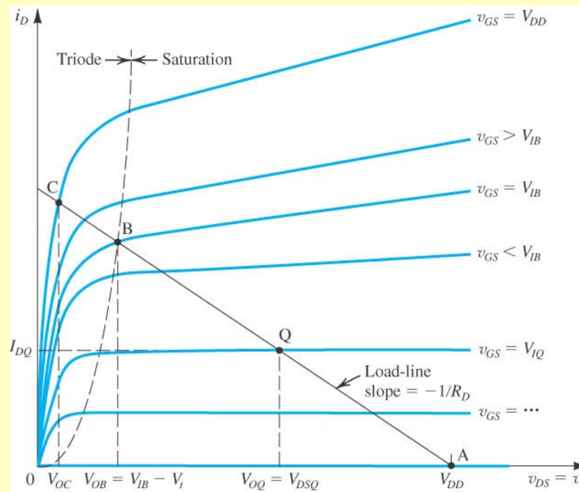


DC Bias + Small-Signal Excitation (cont)

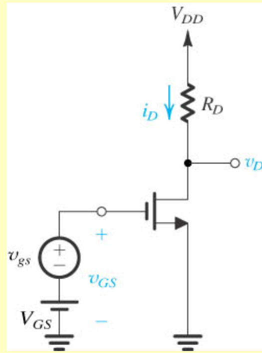


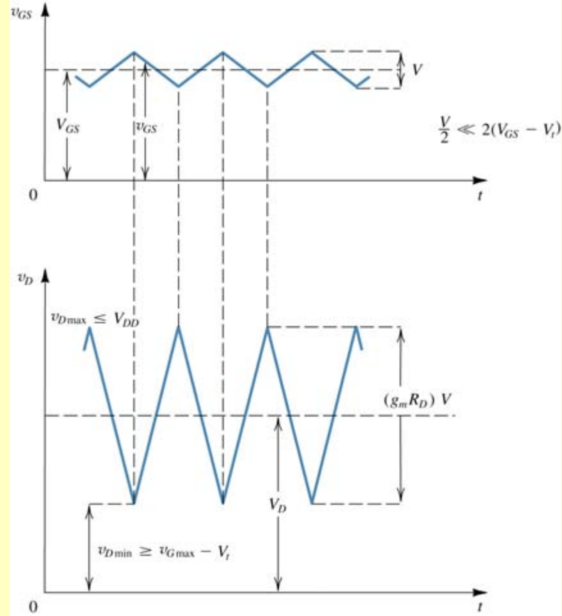
A small variation of v_{gs} can produce a large variation in v_D

Amplification



DC Bias + Small-Signal Excitation (cont)



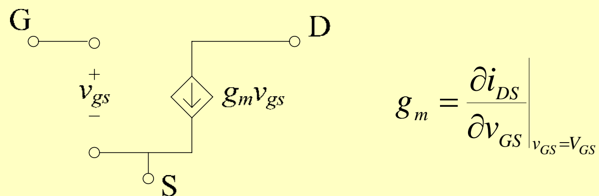


A small variation of v_{gs} can produce a large variation in v_D

→ Amplification

FET Small-Signal Models: Hybrid π Model

- Neglecting the output resistance, r_o



$$g_m = \left.\frac{\partial i_{DS}}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}}$$

JFET:

$$g_m = 2K\,|V_{GS} - V_P\,|$$

$$g_m = \sqrt{4KI_D}$$

$$K = \begin{cases} I_{DSS}/V_P^2 \\ I_{SDS}/V_P^2 \end{cases}$$

MOSFET:

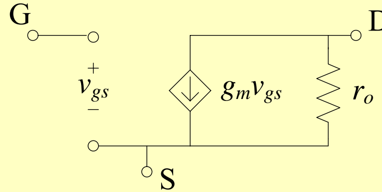
$$g_m = 2K\,|V_{GS} - V_{TH}\,|$$

$$g_m = \sqrt{4KI_D}$$

$$K = \begin{cases} \frac{1}{2}\mu_n C_{OX}\frac{W}{L} \\ \frac{1}{2}\mu_p C_{OX}\frac{W}{L} \end{cases}$$

FET Small-Signal Models: Hybrid π Model (cont)

- Considering the output resistance, r_o



JFET:

$$g_m = \sqrt{4KI_D}$$

$$K = \begin{cases} I_{DSS} / V_P^2 \\ I_{SDS} / V_P^2 \end{cases}$$

$$r_o = V_A / I_D = 1/(\lambda I_D)$$

MOSFET:

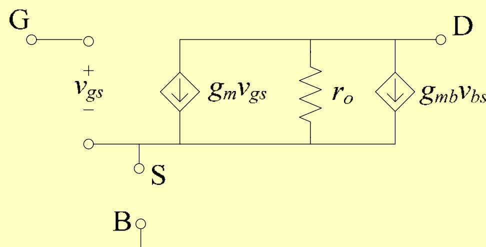
$$g_m = \sqrt{4KI_D}$$

$$K = \begin{cases} \frac{1}{2}\mu_n C_{OX} \frac{W}{L} \\ \frac{1}{2}\mu_p C_{OX} \frac{W}{L} \end{cases}$$

$$r_o = V_A / I_D = 1/(\lambda I_D)$$

FET Small-Signal Models: Hybrid π Model (cont)

- Considering the substrate effect in a MOSFET,



$$g_m = \sqrt{4KI_D}$$

$$K = \begin{cases} \frac{1}{2}\mu_n C_{OX} \frac{W}{L} \\ \frac{1}{2}\mu_p C_{OX} \frac{W}{L} \end{cases}$$

$$r_o = V_A / I_D = 1/(\lambda I_D)$$

$$g_{mb} = \eta g_m$$

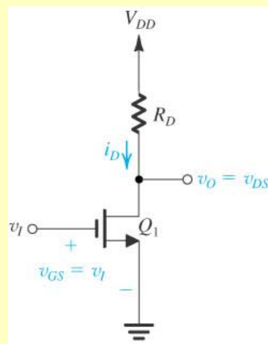
$$\eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}}$$

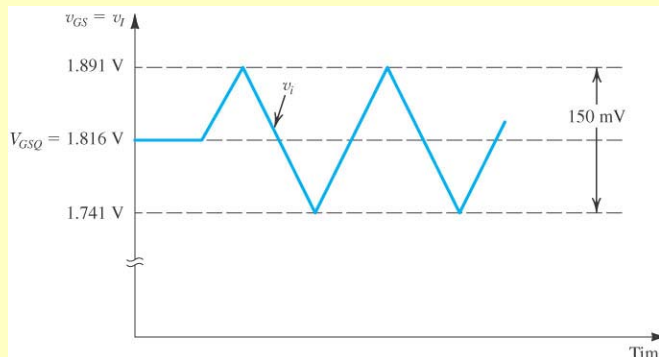
γ is the body effect coefficient

$0.3 \leq \gamma \leq 0.4$

Φ_F is the work function of the silicon substrate or surface potential

DC and Small-Signal Analysis – Example



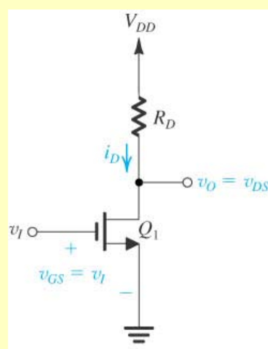


$R_D = 18\text{K}\Omega$
$v_I = 1.816\text{V} + v_i$
$K = 0.5\text{mA/V}^2$
$V_{TH} = 1\text{V}$
$\lambda = 0$

Bias point calculation (DC analysis)

$$I_D = K(V_{GS} - V_{TH})^2$$
$$I_D = 0.5\text{m}(1.816 - 1)^2 = 0.33\text{mA}$$
$$V_{DS} = 10\text{V} - 0.33\text{mA}(18\text{K}\Omega) = 4\text{V}$$

DC and Small-Signal Analysis – Example (cont)



$R_D = 18\text{K}\Omega$
$v_I = 1.816\text{V} + v_i$
$K = 0.5\text{mA/V}^2$
$V_{TH} = 1\text{V}$
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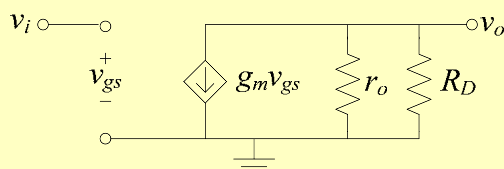
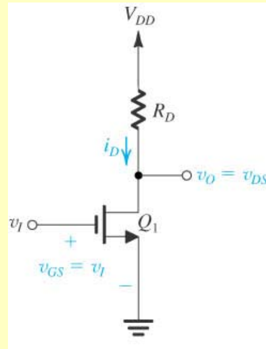
Small-signal analysis (linear analysis)



$$v_o = -g_m v_{gs}(R_D \,\|\, r_o) = -g_m R_D v_i$$
$$A_v = \frac{v_o}{v_i} = -g_m R_D$$
$$g_m = \sqrt{4KI_D} = \sqrt{4(0.5\text{m})(0.33\text{m})} = 0.816\text{m}\Omega^{-1}$$
$$A_v = -(0.816\text{m})(18\text{K}) = -14.69\text{V/V}$$
$$v_o = -14.69(75\text{mV}) = -1.1\text{V}$$
$$v_O = V_{DS} + v_o = 4\text{V} \pm 1.1\text{V}$$

$v_{O\max} = 5.1\text{V}$
$v_{O\min} = 2.9\text{V}$

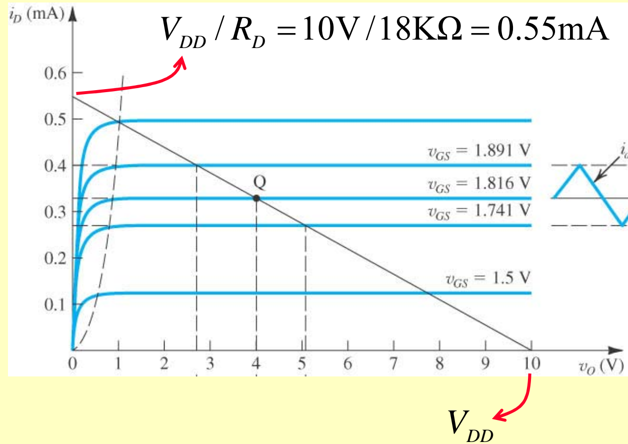
DC and Small-Signal Analysis – Example (cont)



$R_D = 18\text{K}\Omega$
$v_I = 1.816\text{V} + v_i$
$K = 0.5\text{mA/V}^2$
$V_{TH} = 1\text{V}$
$\lambda = 0$

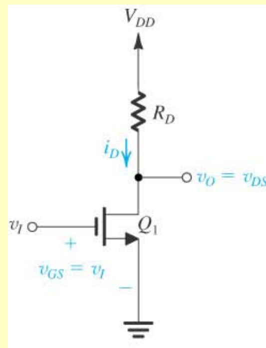
$I_D = 0.33\text{mA}$
$V_{DS} = 4\text{V}$

$V_{DD} / R_D = 10\text{V} / 18\text{K}\Omega = 0.55\text{mA}$



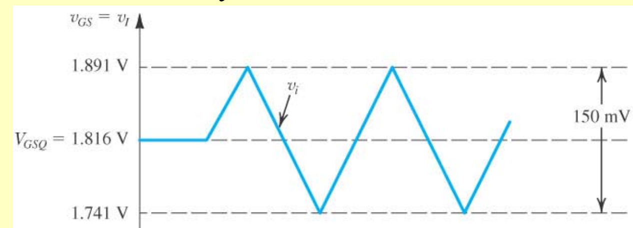
V_{DD}

DC and Small-Signal Analysis – Example (cont)



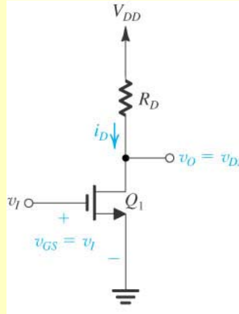
$R_D = 18\text{K}\Omega$
$v_I = 1.816\text{V} + v_i$
$K = 0.5\text{mA/V}^2$
$V_{TH} = 1\text{V}$
$\lambda = 0$

Nonlinear analysis

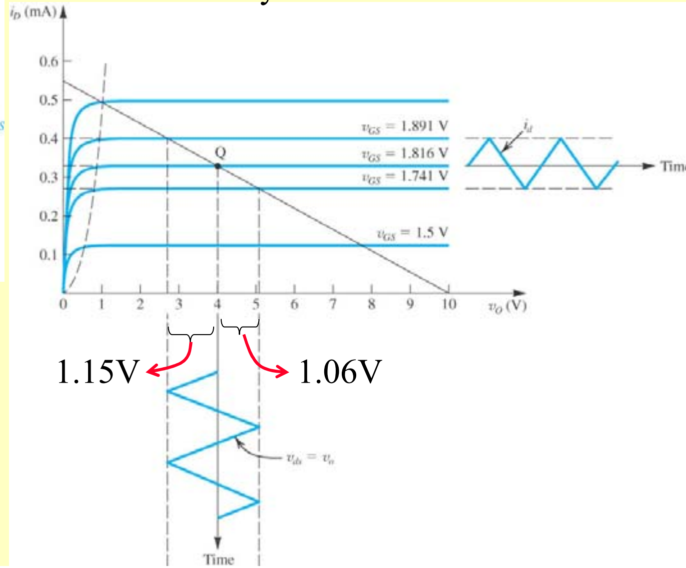


$$I_D = K(V_{GS} - V_{TH})^2$$
$$I_{D\min} = 0.5\text{m}(1.741-1)^2 = 0.274\text{mA}$$
$$I_{D\max} = 0.5\text{m}(1.891-1)^2 = 0.397\text{mA}$$
$$v_{O\max} = V_{DD} - I_{D\min} R_D = 10\text{V} - 4.94\text{V} = 5.06\text{V}$$
$$v_{O\min} = V_{DD} - I_{D\max} R_D = 10\text{V} - 7.146\text{V} = 2.85\text{V}$$

DC and Small-Signal Analysis – Example (cont)



Nonlinear analysis



$R_D = 18\text{K}\Omega$

$v_I = 1.816\text{V} + v_i$

$K = 0.5\text{mA/V}^2$

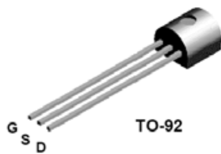
$V_{TH} = 1\text{V}$

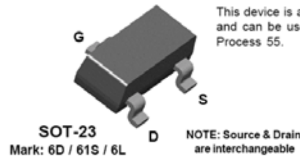
$\lambda = 0$

JFET Manufacturing Data Sheets

2N5457
2N5458
2N5459

MMBF5457
MMBF5458
MMBF5459





N-Channel General Purpose Amplifier

This device is a low level audio amplifier and switching transistors, and can be used for analog switching applications. Sourced from Process 55.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

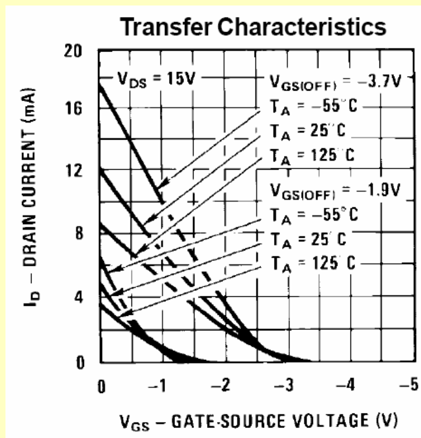
Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	- 25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

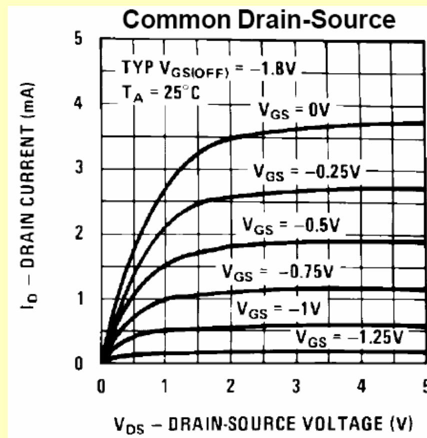
JFET Manufacturing Data Sheets (cont)

Electrical Characteristics TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = 10 μA, V_{DS} = 0	- 25			V
I_{GSS}	Gate Reverse Current	V_{GS} = -15 V, V_{DS} = 0			- 1.0	nA
		V_{GS} = -15 V, V_{DS} = 0, T_A = 100°C			- 200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15 V, I_D = 10 nA **5457**	- 0.5		- 6.0	V
		5458	- 1.0		- 7.0	V
		5459	- 2.0		- 8.0	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15 V, I_D = 100 μA **5457**		- 2.5		V
		V_{DS} = 15 V, I_D = 200 μA **5458**		- 3.5		V
		V_{DS} = 15 V, I_D = 400 μA **5459**		- 4.5		V
ON CHARACTERISTICS						
I_{DSS}	Zero-Gate Voltage Drain Current*	V_{DS} = 15 V, V_{GS} = 0 **5457**	1.0	3.0	5.0	mA
		5458	2.0	6.0	9.0	mA
		5459	4.0	9.0	16	mA
SMALL SIGNAL CHARACTERISTICS						
g_{fs}	Forward Transfer Conductance*	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz				
		5457	1000		5000	μmhos
		5458	1500		5500	μmhos
		5459	2000		6000	μmhos
g_{os}	Output Conductance*	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz		10	50	μmhos
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz		4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz		1.5	3.0	pF
NF	Noise Figure	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz, R_G = 1.0 megohm, BW = 1.0 Hz			3.0	dB

JFET Manufacturing Data Sheets (cont)

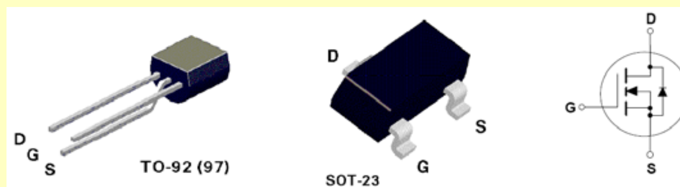




MOSFET Manufacturing Data Sheets

FAIRCHILD SEMICONDUCTOR™

BS170 / MMBF170
N-Channel Enhancement Mode Field Effect Transistor



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq$ 1MΩ)	60		V
V_{GSS}	Gate-Source Voltage	± 20		V
I_D	Drain Current - Continuous	500	500	mA
	- Pulsed	1200	800	
P_D	Maximum Power Dissipation	830	300	mW
	Derate Above 25°C	6.6	2.4	mW/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300		°C

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MOSFET Manufacturing Data Sheets (cont)

FAIRCHILD SEMICONDUCTOR™

BS170 / MMBF170
N-Channel Enhancement Mode Field Effect Transistor

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 100 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25 V, V_{GS} = 0 V	All			0.5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15 V, V_{DS} = 0 V	All			10	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	All	0.8	2.1	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 200 mA	All		1.2	5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	BS170		320		mS
		$V_{DS} \geq$ 2 $V_{DS(on)}$, I_D = 200 mA	MMBF170		320		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	All		24	40	pF
C_{oss}	Output Capacitance		All		17	30	pF
C_{rss}	Reverse Transfer Capacitance		All		7	10	pF

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MOSFET Manufacturing Data Sheets (cont)

BS170 / MMBF170
N-Channel Enhancement Mode Field Effect Transistor

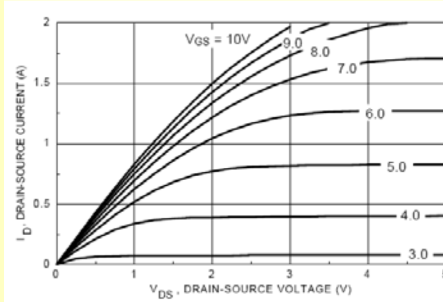

Figure 1. On-Region Characteristics.

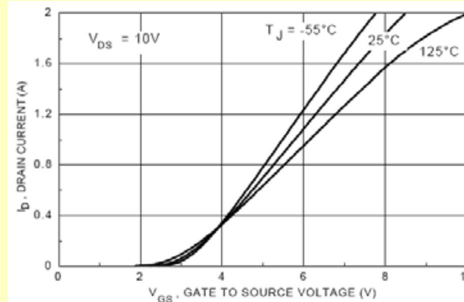

Figure 5. Transfer Characteristics.

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MOSFET Manufacturing Data Sheets (cont)

BS170 / MMBF170
N-Channel Enhancement Mode Field Effect Transistor

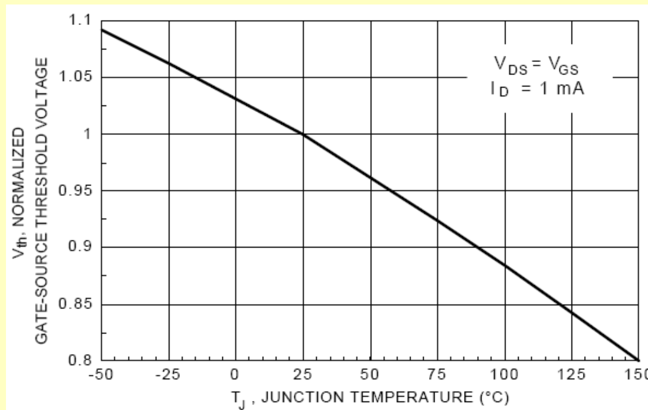

Figure 6. Gate Threshold Variation with Temperature.

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