Introduction to CMOS Logic Design

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Most figures of this presentation were taken from the instructional resources of the following textbook:

A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. New York, NY: Oxford University Press, 2003.

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Outline

- Technologies and logic families
- Transfer characteristics
- Transition and propagation times
- Modeling CMOS Inverters
- Matched CMOS Inverters
- Dynamic operation of CMOS inverters
- General structure of CMOS logic circuits
- Examples of CMOS logic gates
- Dimensioning transistors in CMOS logic circuits

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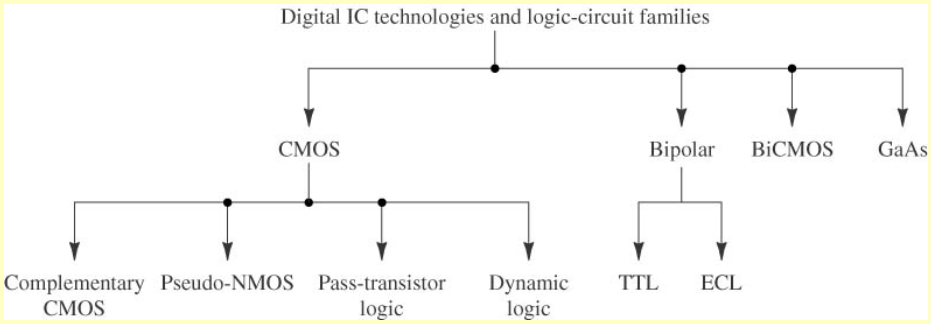
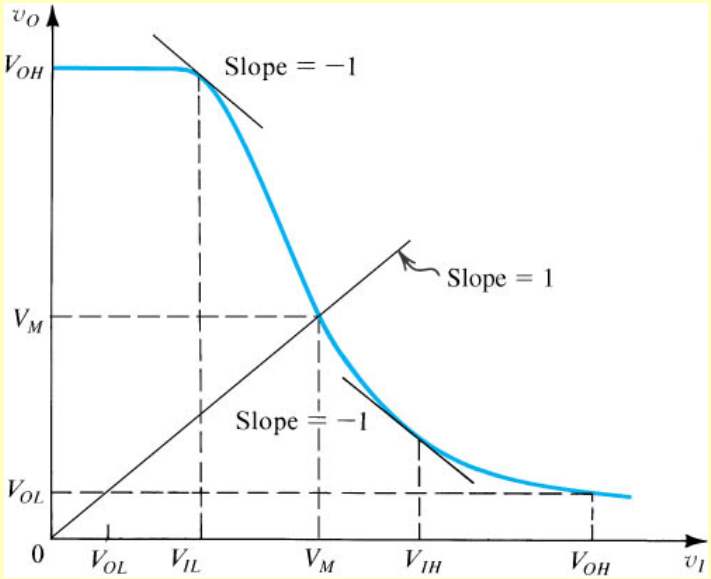
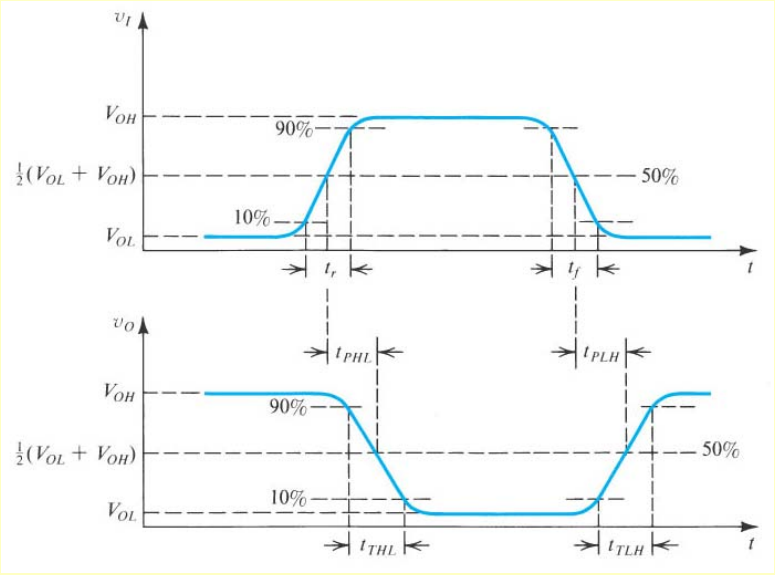
Digital IC Technologies and Logic Families



Typical Inverter Voltage Transfer Characteristic



Transition Times and Propagation Delays



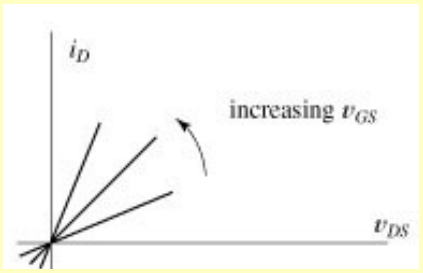
Ohmic Region (review)

If $v_{GS} \geq V_{TH}$ and v_{DS} is small ($v_{DS} << v_{GS} - V_{TH}$),

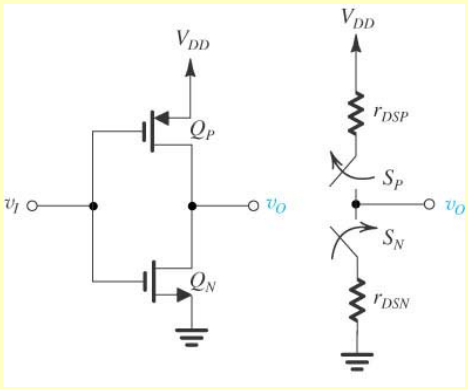
→ ohmic region or deep triode region

$$r_{DS} = \frac{v_{DS}}{i_{DS}} \approx \frac{1}{\mu_n C_{OX} \frac{W}{L}(v_{GS} - V_{TH})} = \frac{1}{2K(v_{GS} - V_{TH})}$$

for v_{DS} small

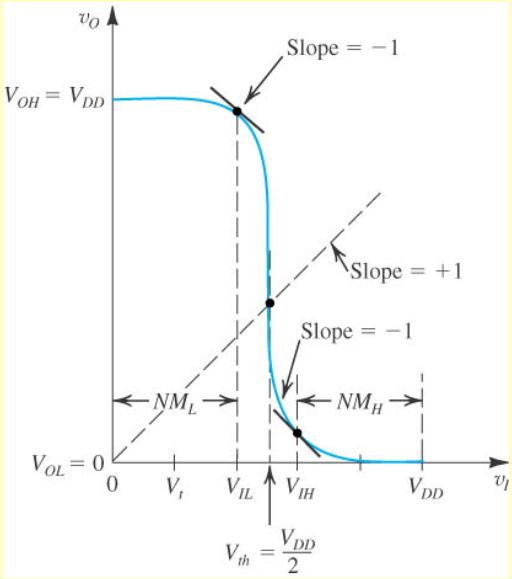


A CMOS Inverter

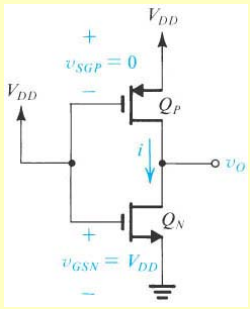


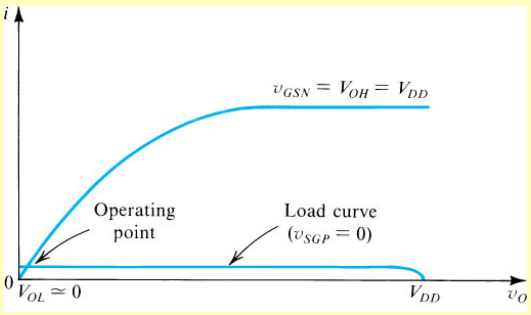
$$r_{DSN} \approx \frac{1}{\mu_n C_{OX} \frac{W_n}{L_n}(v_{GS} - V_{THn})} \qquad r_{DSP} \approx \frac{1}{\mu_p C_{OX} \frac{W_p}{L_p}(v_{SG} - |V_{THp}|)}$$

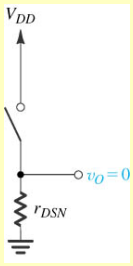
Transfer Characteristic of a Matched Inverter



A CMOS Inverter when $v_I = V_{DD}$

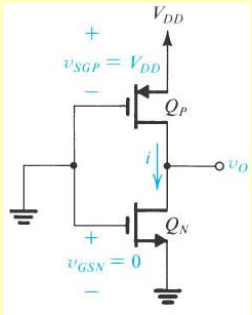


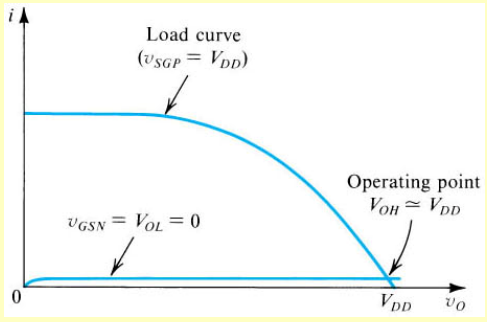


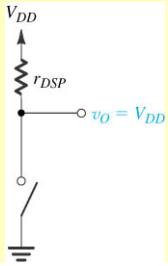


$$r_{DSN} \approx \frac{1}{\mu_n C_{OX} \frac{W_n}{L_n}(V_{DD} - V_{THn})}$$

A CMOS Inverter when $v_I = 0$V

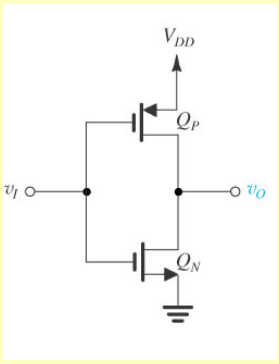


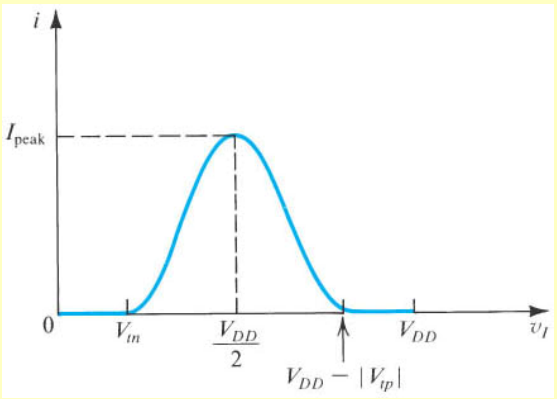




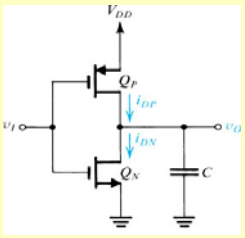
$$r_{DSP} \approx \frac{1}{\mu_p C_{OX} \frac{W_p}{L_p}(v_{DD} - |V_{THp}|)}$$

Inverter Current *vs* Input Voltage

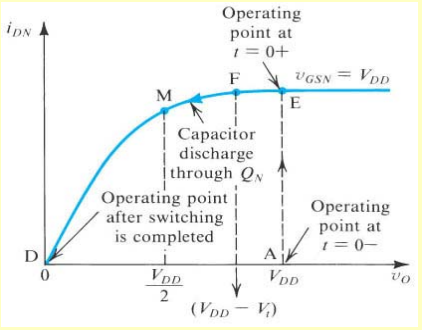


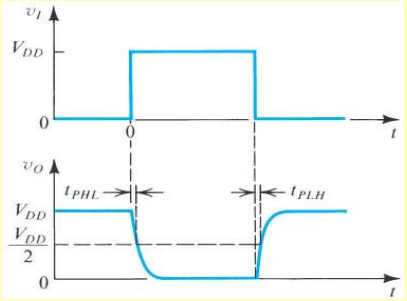


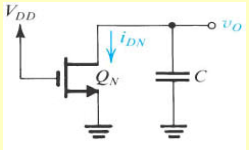
Dynamic Operation with a Capacitive Load



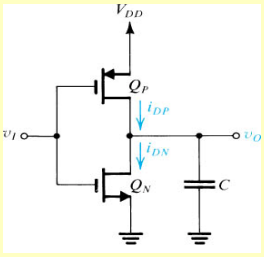
When v_I switches from 0 to V_{DD}:

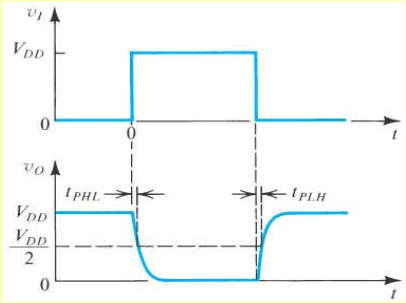






Power Consumption with a Capacitive Load





The energy stored in C is:

$$W_C = \frac{1}{2}C(v_O(t))^2$$

when $t = 0^-$ (C is fully charged)

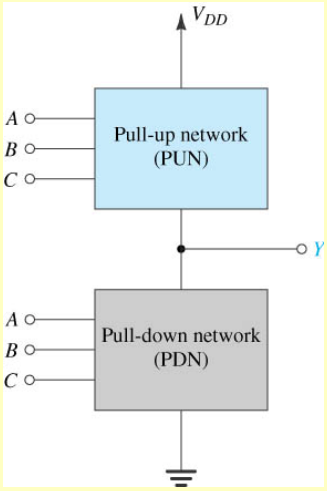
$$W_C(t = 0^-) = \frac{1}{2}CV_{DD}^2$$

which is the energy that must be dissipated by Q_N when C is discharged, and by Q_P when C is charged. Hence, the total energy per cycle is:

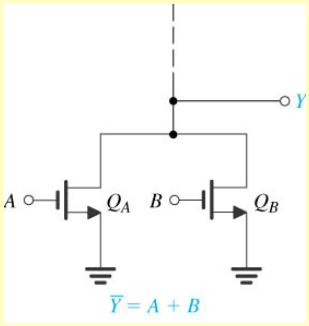
$$W_{total} = CV_{DD}^2 = \int_0^T P_D dt = P_D T$$

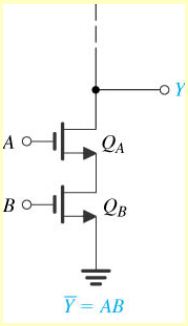
$$P_D = fCV_{DD}^2$$

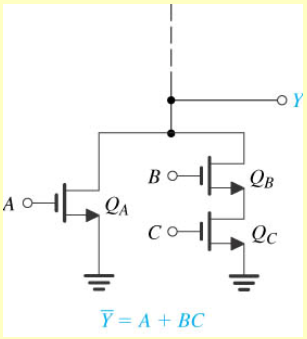
General Structure of CMOS Logic Circuits



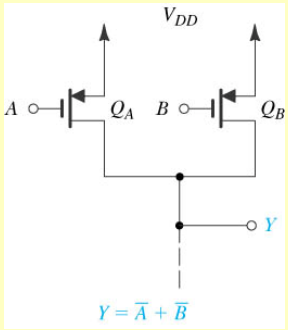
Pull-Down Networks - Examples

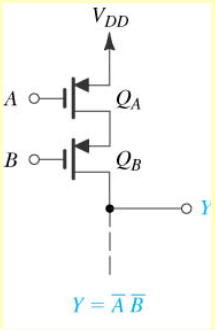


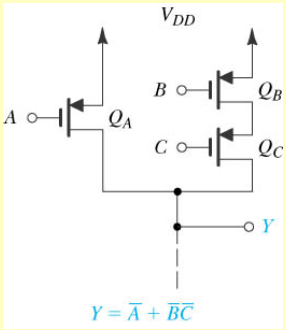




Pull-Up Networks - Examples







Examples…

Dimensioning…