Analog Electronic Devices
(ESI038 / SE047)

Lab Experiment 5:
Introduction to CMOS Logic Design

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Objectives

The objectives of this lab experiment are:

a) to design a basic combinational logic circuit using CMOS technology

b) to simulate the electrical performance of a digital circuit at the transistor level.

Components and Instrumentation

A circuit simulation software: WinSpice, OrCad, Electronic Work Bench, or something similar.

Theoretical Procedure

1. Using CMOS transistors, design a circuit to implement the logic function $Y = \mathrm{not}[A+B(C+D)]$.
2. Take the channel length $L = 1\mu m$ and the threshold voltage $V_{THn} = |V_{THp}| = 0.5V$ for all transistors. Use $V_{DD} = 3.3V$. Taking $kp_n = \mu_n C_{ox} = 100\mu A/V^2$ and $kp_p = \mu_p C_{ox} = 50\mu A/V^2$, choose the channel width W of each transistor to achieve a suitable performance.

Simulation Procedure

1. Simulate your complete logic circuit using SPICE:
   a. Make sure each E-MOS transistor is implemented in SPICE with the correct physical dimensions (W and L) and parameters (V_{TH} and kp).
   b. Perform a transient simulation using periodic pulsed signals for the inputs A, B, C and D, so that you can test the logic function.

Report

Write a report including all the theoretical and simulation procedures as well as your conclusions. Since it is a design problem, it is important to make explicit all the calculations during the design process. The report must include the schematic of the complete final circuit, and the waveforms obtained during the simulation.

Deadline and Assessment

The deadline for submitting the report is on Friday, May 11, 2007. The report can be written either in English or in Spanish.

This lab experiment can be realized in teams of up to 3 students. The evaluation of the report will be as follows:

Quality of the report	30%
Accuracy of the theoretical analysis	30%
Simulation procedures	40%

If the report is written in acceptable English, an extra 10% can be granted.

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