Signal Integrity

Second ITESO-Intel International Workshop on Signal Integrity I³WSI-2006

Signal Integrity is emerging as a well-defined self-contained discipline. It can be defined as an engineering practice that aims at ensuring reliable high-speed data transmission and reception, without polluting the electromagnetic spectrum and without damaging any device. Signal Integrity effectively combines concepts and techniques from the following more traditional disciplines: microwave and RF engineering; electromagnetics; physical design; analog electronics; communications; and digital design.

Our second ITESO-Intel International Workshop on Signal Integrity (I³WSI-2006) aims at reviewing the fundamentals as well as the state-of-the-art techniques related to modeling, testing, circuit and EM simulation and design techniques of high-speed interconnects for optimal signal integrity performance.

The I³WSI-2006 will bring together the foremost researchers and practitioners in the field of signal integrity and high-speed interconnects, including senior industrial innovators and prestigious academic researchers. We blend technological aspects of wide applicability, simulation and design procedures currently applied in research and development centers, and measuring tools and testing procedures for high-speed design purposes.

ITESO
UNIVERSIDAD JESUITA DE GUADALAJARA

intel

IEEE

Technical Program

Richard Mellitz
Intel Corporation, Columbia, South Carolina
Assumptions: History and Birth of Signal Integrity

Howard Heck
Intel Corporate Technology Group, Hillsboro, Oregon
SI Modeling Requirements For Microprocessor Systems: Past, Present & Future

James C. Rautio, Fellow IEEE
Sonnet Software, Inc.
Electromagnetic Analysis and Signal Integrity

John W. Bandler, Fellow IEEE
Bandler Corporation and McMaster University, Ontario, Canada
Space Mapping Technology for EM-Based Modeling and Optimization: The State Of The Art

Zoltan J. Cendes, Fellow IEEE
Ansoft Corporation
Simulation and Design Management for High-Speed Interconnects

Ram Achar
Carleton University, Ottawa, Canada
Advances in the Modeling and Simulation of High-speed Interconnects

Paul Huray
University of South Carolina
3-D Model For Surface Roughness Loss

Telesphor Kamgaing
Intel Corporation, Chandler, Arizona
Electromagnetic Band-Gap Structures for Mitigation of Switching Noise in Power Delivery Networks of High-Speed Circuits

James C. Rautio, Fellow IEEE
Sonnet Software, Inc.
IEEE MTT-S Distinguished Lecture: The Life of James Clerk Maxwell

Kevin P. Slattery
Intel Corporation, Hillsboro, Oregon
An EMI Analysis of Digital Display Symbols

José Ernesto Rayas-Sánchez and Vladimir Gutiérrez-Ayala
Instituto Tecnológico y de Estudios Superiores de Occidente (ITESO), Guadalajara, Mexico
Towards the Optimal Design of Substrate Integrated Waveguide Interconnects using Full-wave Electromagnetic Simulators

Reydezel Torres-Torres[1], Gerardo Romo[1], Bryce Horine[2], Adán Sánchez[1] and Howard Heck[2]
[1]Intel Mexico Research Center
[2] Platform Technologies Laboratory, Intel Corporation, Hillsboro, Oregon
Full Characterization of Substrate Integrated Waveguides from S-Parameter Measurements

Edmundo A. Gutiérrez-D.
Intel-SRCM, Guadalajara, Mexico
Simulation and Analysis of on-chip RF Emission of IC Interconnects

Víctor Avendaño Fernández[1] and Víctor Champac[2]
[1]Freescale Mixed-Signal Technology Center, Guadalajara, Mexico
[2] Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Puebla, Mexico
Analysis and Verification for Integrity Issues in Digital Signals

Robert Hanson
Americom Seminars, Inc.
Tutorial: Overview of High-Speed Digital Design Concerns

Guadalajara, Mexico
October 5-6, 2006
http://wsi.iteso.mx

Fees (Mexican Pesos):

Professional IEEE	$3,800.00*
Student IEEE	$1,500.00*
Student with IEEE registration	$1,750.00*
Professional	$4,900.00*
Student	$2,600.00*

** Includes lunch and coffee break services for both days*

Second ITESO-Intel International Workshop on Signal Integrity (I3WSI)
I3WSI-2006 Technical Program
October 5-6, 2006

Time	Thursday 5
7:30 – 8:30 AM	Registration
8:30 – 9:00 AM	Welcome and opening remarks
9:00 – 9:40 AM	Richard Mellitz Intel Corporation, Columbia, South Carolina ***Assumptions: History and Birth of Signal Integrity***
9:40 – 10:20 AM	Howard Heck Intel Corporate Technology Group, Hillsboro, Oregon ***SI Modeling Requirements For Microprocessor Systems: Past, Present & Future***
10:20 – 10:35 AM	Coffee break
10:35 – 11:15 AM	Session TH3
11:15 – 11:55 AM	Session TH4
11:55 – 12:10 PM	Coffee break
12:10 – 12:50 PM	Session TH5
12:50 – 1:30 PM	Session TH6
1:30 – 3:00 PM	Lunch
3:00 – 3:40 PM	Session TH7
3:40 – 4:20 PM	Session TH8
4:20 – 5:00 PM	Session TH9
5:00 – 5:20 PM	Coffee break
5:20 – 6:50 PM	IEEE MTT-S Distinguished Lecture
6:50 – 8:00 PM	Cocktail

Time	Friday 6
7:30 – 8:30 AM	Registration
8:30 – 9:00 AM	Session F1
9:00 – 9:30 AM	Session F2
9:30 – 9:40 AM	Coffee break
9:40 – 10:10 AM	Session F3
10:10 – 10:40 AM	Session F4
10:40 – 11:00 AM	Coffee break
11:00 – 2:30 PM	Tutorial
2:30 – 2:35 PM	Closing remarks
2:35 – 4:35 PM	Lunch
4:35 – 7 PM	Social event

Thursday 5		
Session	**Author(s), Affiliation & *Title***	**Abstract**
TH1	Richard Mellitz Intel Corporation, Columbia, South Carolina ***Assumptions: History and Birth of Signal Integrity***	Imaging filling your car with a tank of gas and it never ran out. Ridiculous? Well consider an electrical engineer building a model for a circuit and using a battery to energize the circuit. Of course is it understood that it's just a convenience for analysis but at some level all engineers make assumptions. Assumptions are unearthed by the plow of technology advancement. Often these have become the "Achilles Heel" of signal integrity analysis and consequently product design. This chronological anthology will travel though a progression of digital design challenges and assumption. There was a time when the number of loads was the only critical signaling design consideration. A lot of assumptions were made that seem sophomoric or even infantile by today standards. We will unearth these assumptions as the presentation moves through the decades of digital design. Do you remember when we first started thinking about return path or via coupling? Why did these phenomena emerge as problematic SI issues? The answer is assumptions. These signaling design challenges fostered the growth of Signal Integrity as an engineering discipline. The presentation will leave you with the challenge and mission to unearth the critical assumptions we are making that could become the next chink in our armor.
TH2	Howard Heck Intel Corporate Technology Group, Hillsboro, Oregon ***SI Modeling Requirements for Microprocessor Systems: Past, Present & Future***	Moore's Law has been the fundamental driving force behind the PC industry and the microprocessor for nearly thirty years, providing a doubling in system performance approximately every two years. In addition to the more visible measures (e.g. transistors per chip), staying on the Moore's Law trend drives exponential growth in inter-chip signaling bandwidths. Meeting this demand places pressure on interconnect modeling to provide repeated accuracy improvements while handling increased frequencies. This presentation will examine the requirements for interconnect models, taking a historical view to demonstrate the growth in modeling requirements through time, and to project future requirements while suggesting areas for high speed modeling research, covering specific modeling issues for printed circuit boards and connectors, such as: a) copper surface roughness and effects on skin effect loss; b) FR4 dielectric weave construction and effects on mode conversion in differential signals; c) 3D modeling of plated through holes and edge card connectors; d) dielectric losses 40+ GHz.
TH3	James C. Rautio, Fellow IEEE Sonnet Software, Inc. ***Electromagnetic Analysis and Signal Integrity***	Electromagnetic (EM) analysis allows a first-principles evaluation of high speed digital interconnect. Issues such as cross-talk, signal delay, transmission loss, impedance mismatch, and reflection are evaluated quantitatively. This presentation starts with an overview of different types of EM analysis and their relative advantages and disadvantages. Next, detail is provided about a specific type of EM analysis, planar Method of Moments, in both unshielded and shielded environments. The basic approach in both techniques is to calculate scattering parameters (S-parameters) over a range of frequencies. For signal integrity work, these S-parameters are then typically converted into a broad band SPICE compatible lumped model. The lumped model is then used to quantify signal integrity issues. Problems with this approach include the fact the SPICE model is often unstable, especially for complicated structures with large numbers of ports. Research underway at this writing suggests that the instability is due to non-physical EM analysis error present to some degree in all EM analyses. Even very small error of the wrong kind can yield an unstable lumped model. We explore sources of these errors and show how to reduce these errors so that circuits of practical complexity can be successfully modeled. This work comes from an RF/microwave design viewpoint. No equations of any kind are used, all theory is presented in a purely conceptual, physical manner.
TH4	John W. Bandler, Fellow IEEE, Qingsha S. Cheng, and Slawomir Koziel Bandler Corporation and McMaster University, Ontario, Canada ***Space Mapping Technology for EM-Based Modeling and Optimization: The State Of The Art***	We review new research developments in the space mapping and space-mapping-based surrogate modeling concepts. The aim of space mapping is to achieve satisfactory engineering models and design solutions with minimal numbers of computationally expensive high fidelity or "fine" model evaluations. Space mapping optimization procedures iteratively update and optimize suitable surrogates based on fast, physically-based "coarse" or low-fidelity models. We explain our space mapping techniques through simple and intuitive everyday illustrations. We describe a space mapping technology involving so-called input, implicit, frequency, derivative, interpolation, and output mappings. We introduce implementations of space mapping using widely available commercial software as well as our newly developed SMF software system. We review significant applications in engineering model enhancement and design optimization, emphasizing the RF and microwave arena.
TH5	Zoltan J. Cendes, Fellow IEEE Ansoft Corporation ***Simulation and Design Management for High-Speed Interconnects***	Engineers designing servers, storage devices, multimedia PCs, entertainment systems, and telecom systems have driven an industry trend to replace legacy shared parallel buses with high-speed point-to-point serial buses. Standard interfaces like XAUI, XFI, Serial ATA, PCI Express, HDMI, and FB-DIMM have emerged to provide greater throughput using serial signaling rates of 2.5 to 10 Gb/s. While this trend has greatly reduced the number of traces and connections within the system, it has created new challenges for board designers when considering implementation with multiple connectors, transmission lines, vias, IC packaging, and transceiver circuits. Reliable signal transmission across a host board or between daughter cards on a backplane at GHz speeds compels adoption of new strategies and tools. Intel and Ansoft have teamed to define a Reference Flow for High-speed Serial Interconnect. This joint effort leverages Intel's expertise in designing and developing high-speed serial interconnect technology and standards, and combines that expertise with advanced circuit simulation and

		electromagnetic extraction tools from Ansoft. A unified design flow that includes physics based models for interconnects combined with advanced circuit simulation technology provides the platform for modern multi-gigabit design. Although traditional electronic design automation (EDA) tools can be used for some channel analyses, traditional design solutions with disparate solvers, creates challenges for design management and is highly error prone. This paper describes the methods used to reliably characterize and manage complex serial channel designs. Circuits and interconnect examples from PCI Express channel design will be used as a vehicle to demonstrate the flow.
TH6	Ram Achar Carleton University, Ottawa, Canada ***Advances in the Modeling and Simulation of High-speed Interconnects***	The intense drive for signal integrity has been at the forefront of rapid and new development in CAD algorithms. With increasing demands for high signal speeds coupled with decreasing feature sizes, interconnect effects such as signal delay, distortion and crosstalk become the dominant factors limiting overall performance of high-speed systems. On the other hand, interconnect structures can be diverse and present at any of the hierarchical packaging levels including integrated circuits, printed circuit boards, multi-chip modules and backplanes. If not considered during the design stage, interconnect effects can cause failed designs. Since extra iterations in the design cycle are costly, accurate prediction of these effects is a necessity in high-speed designs. Although conventional CAD tools such as SPICE are used routinely by many engineers for analog simulation and general circuit analysis, these tools do not handle adequately the new emerging challenges of interconnect effects. In this talk, an overview of the emerging area of signal integrity, high-frequency issues and the related modeling/simulation difficulties will be discussed. It will present an overview as well as the most recent advances in the interconnect modeling/simulation strategies with emphasis on distributed multiconductor transmission lines and tabulated (scattering) type of subnetworks. Various levels of interconnect modeling will be considered and the applications cover wide spectrum of on-chip, multichip, packages, printed circuit boards, and backplanes/connectors.
TH7	Paul Huray University of South Carolina ***3-D Model For Surface Roughness Loss***	PCB manufacturers make conducting trace surfaces rough to enhance adhesion but the roughness also causes substantial power loss. As CPU speeds increase beyond their present level, designers need a method to predict those losses at higher frequencies to determine if an alternate means of processing will be required for signal integrity. A team of researchers at Intel has studied the effects of rough surfaces with measurements to 67 GHz, and with simulation and theory to 100 GHz. The theory requires a 3-D model of surface roughness in order to predict losses at the higher rates. The model will be presented and compared to measurements and simulation.
TH8	Telesphor Kamgaing Intel Corporation, Chandler, Arizona ***Electromagnetic Band-Gap Structures for Mitigation of Switching Noise in Power Delivery Networks of High-Speed Circuits***	Moore's law continues to drive the number of transistors in the microprocessor chip. At the same time there is a continuous increase in the clock frequency. The combination of these two parameters contributes to the increase of switching noise associated with the simultaneous switching of thousands to millions of transistors. In this presentation, we will discuss the concept of utilizing electromagnetic band-gap structures for the mitigation of such noise. PCB and package level implementations of this novel solution will be addressed. In addition, novel multiband Inductance-Enhanced EBG (IE-EBG), requiring only sub-millimeter dimensions for low-GHz applications are designed and fully characterized in standard multilayer organic package substrate. This dimensional compatibility with today's packaging technology is an indication that IE-EBG can be used for other applications such as commercial wireless communication systems.
TH9	Kevin P. Slattery Intel Corporation, Hillsboro, Oregon ***An EMI Analysis of Digital Display Symbols***	Digital display frames and their associated symbols have spectra that fall somewhere between a purely repetitive symbol sequence such as a clock, and a purely random sequence of a finite set of symbols such as a Pseudo-random bit stream (PRBS). This paper describes a method whereby a selected set of display symbols can be ranked according to the expected EMI impact of their bit structure. The analysis will show that out of a given symbol set a subset of the symbols should be used for highly repetitive sequences, such as blanking, to produce emissions that can be lower by up to 10 dB.
MTT-S	James C. Rautio, Fellow IEEE Sonnet Software, Inc. ***IEEE MTT-S Distinguished Lecture: The Life of James Clerk Maxwell***	James Clerk Maxwell stands shoulder to shoulder with Newton and Einstein, yet even those of us who have spent decades working with Maxwell's equations are almost totally unfamiliar with his life and times. This presentation, from the viewpoint of a microwave engineer, draws on many sources in providing an understanding of James Maxwell himself. What was Maxwell like as an infant? What was the tragedy at eight years old that profoundly influenced his life? What unique means of transportation did young Maxwell use to escape a cruel tutor? What memorable event occurred on his first day of school? When did he publish his first papers, and what were they about? What did Maxwell have to do with the rings of Saturn? Why did he lose his job as a professor? Why did he have a hard time getting another job? What was his wife like? What is Maxwell's legacy to us? The answers to these questions provide insight into Maxwell the person and add an extra dimension to those four simple equations we have studied ever since. There are no equations in this presentation. The presentation is appropriate for anyone with a general interest in the origins of modern physics. For electronic handouts for the lecture, visit www.sonnetsoftware.com and click on the large Distinguished Microwave Lecture Series" button at the bottom of the "News" section.

Friday 6		
Session	**Author(s), Affiliation and *Title***	**Abstract**
F1	José Ernesto Rayas-Sánchez and Vladimir Gutiérrez-Ayala ITESO, Guadalajara, Mexico ***Towards the Optimal Design of Substrate Integrated Waveguide Interconnects using Full-wave Electromagnetic Simulators***	Rectangular waveguides are very suitable for realizing high-performance microwave passive components due to their high Q-factor and high power capacity. However, conventional waveguides are bulky and difficult to embed in typical multilayer printed circuit boards (PCB). In the microwave range, the physical dimensions of planar transmission lines and waveguides are quite different, imposing the need of complex transition structures that usually require high-precision manufacturing processes and even some kind of tuning, making them unsuitable for low-cost massive-production PCB structures. Substrate integrated circuits have been proposed for fabrication of low-cost high-performance passive circuits such as filters, resonators, couplers, power dividers, circulators and antennas. These structures aim at exploiting the advantages of both rectangular waveguides and microstrip lines (high Q-factor, high power capacity, low-cost, small size and simplicity of integration). Substrate integrated waveguide (SIW) structures are promising candidates for a new generation of low-cost PCB structures for high-speed digital applications, given their simplicity and adequacy for planar and multilayer structures. In this presentation we demonstrate, by using full-wave electromagnetic (EM) simulators, the limitations of conventional planar interconnect structures, and show in an evolutionary fashion the improvement in performance of low-cost state-of-the-art geometries, aiming at establishing a knowledge base towards the optimization of SIW interconnects.
F2	Reydezel Torres-Torres[1], Gerardo Romo[1], Bryce Horine[2], Adán Sánchez[1], Howard Heck[2] [1] Intel Mexico Research Center [2] Intel Corporation, Hillsboro, Oregon ***Full Characterization of Substrate Integrated Waveguides from S-Parameter Measurements***	A complete characterization of substrate integrated waveguide (SIW) structures from S-parameter measurements has been performed. We have experimentally determined the complex propagation constant and the characteristic impedance of an SIW, and also the efficiency of different adapters used to launch the signals into the waveguide. After performing S-parameter measurements on complete SIW-based channels using different adapters, our de-embedding method is applied to produce a segmented model. That is, data is extracted which represents, separately, the effects associated with the intrinsic waveguide from those corresponding to the launch structures. This allows a careful assessment of the losses which take place on each segment. After a detailed analysis, it is observed that the most significant losses in an SIW structure are associated with the adapters since a very low insertion loss is presented in a homogeneous section of waveguide. These results show that the implementation of a low loss SIW-based interconnection channel for high speed digital applications is quite feasible, but requires a careful design of the launch structures.
F3	Edmundo A. Gutiérrez-D. Intel-SRCM, Guadalajara, Mexico ***Simulation and Analysis of on-chip RF Emission of IC Interconnects***	This paper introduces an analysis and simulation of electromagnetic radiation originated from interconnection lines of integrated circuits (IC). The impact of the signal frequency, the bias conditions, and the geometry and layout of the interconnection structure is also addressed. This analysis is used to understand the potential RF interference that may be caused by this emission, and also to predict on-chip signal integrity.
F4	Victor Avendaño Fernández[1] Víctor Champac[2] Joan Figueras[3] [1] Freescale Mixed-Signal Technology Center, Guadalajara, México [2] INAOE), Puebla, México [3] Universitat Politecnica de Catalunya- Barcelona, Spain ***Analysis and Verification for Integrity Issues in Digital Signals***	Advanced technologies allow to integrate several functional blocks, named each one intellectual property (IP), into the same chip. In this type of circuits, System on Chip (SoC), several analogue and digital blocks are interacting together into the same IC. Thanks to this features, today it is possible to have high performance systems (microprocessors, LAN's, SERDES, DSP's) working at very high frequencies. The on-chip interconnect density into these actual SoCs is huge and their impact on signal integrity can be critical for the system performance. This work shows how an excessive inductive coupling between on-chip interconnects could produce signal integrity violations. Noise (overshoots) in digital signals are analyzed by extracting the dominant poles from the characteristic equation of the interconnect, also acceptable and non-acceptable signal integrity regions have been established by using the pole loci obtained from the signal under verification (SUV) and for different interconnects lengths. Also the work presents experimental results for the proposed methodology to verify signal integrity violations. Two types of sensors have been fabricated, one type to monitor overshoots and the other type to monitor undershoots in digital signals. Each monitor works under the coherent sampling scheme to verify the SUV. Silicon results for verifying SUV at frequencies rates of 320MHz, 640Mhz, and 917Mhz applying two different sampling frequencies are also presented.

Session	Author(s), Affiliation and *Title*	Description and General Contents
Tutorial	Robert Hanson Americom Seminars, Inc. ***Overview of High-Speed Digital Design Concerns***	The speed of today's logic devices mandates that the interconnects on PCBs must meet the high switching rise/fall times of these devices. Switching edges are in the 200ps to 300ps range, and some devices have edges that have reached the 17ps rate. This has resulted in high-speed design problems such as: a) A lack of control over impedance and reflections; b) Crosstalk and bypassing failures; c) Time delays, false triggering, and reflections; d) Failure to meet EMI and FCC requirements. It is the edge rate, not the frequency, which exacerbates this problem. So, even if your design is for moderate frequency, the edge rates can cause these designs to reflect the high-speed effects. The purpose of this course is to provide you with the knowledge to do it right the first time. The course provides tools for recognizing the problems with any proposed high-speed design. Design rules and design processes are taught that ensure the PCB will function properly at the prototype stage. The course emphasizes cost competitive design without sacrificing high-speed integrity.

Signal Integrity

CALL FOR PAPERS

The Technical Program Committee of the **2nd ITESO-Intel International Workshop on Signal Integrity (I3WSI-2006)**, wishes to invite technical papers for the 2006 issue of the event, which will be held during October 5-6, 2006, in Guadalajara, Mexico.

The I3WSI-2006 will bring together the foremost researchers and practitioners in the field of signal integrity and high-speed interconnects, including senior Intel innovators and prestigious academic researchers. We blend technological aspects of wide applicability, simulation and design procedures currently applied in research and development centers, and measuring tools and testing procedures for high-speed design purposes.

The I3WSI-2006 is requiring original work in state-of-the-art modeling, testing, simulation and design techniques of high-speed interconnects for optimal signal integrity performance.

Submission of papers: Manuscripts of the final paper (4-page length) must be submitted to the Technical Program Committee in PDF format for consideration as part of the technical program (no hard copies accepted). The paper must include: the title, name(s) and affiliations of the author(s): the mailing address, telephone and fax numbers, and the e-mail address of the corresponding author if available. The paper should clearly state the purpose and contribution of the work, specific results and methods used. Manuscripts should conform to formats and requirements for regular IEEE papers: ***http://wsi.iteso.mx/template***

Deadlines:

Paper submission: **June 12, 2006**
Notification of acceptance: **July 3, 2006**

Technical Program Committee:

Dr. José Ernesto Rayas-Sánchez
ITESO
Tel: +5233 3669 3434 ext. 3096
E-mail: erayas@iteso.mx

Dr. Juan Manuel Hernández Cid
ITESO
Tel: +5233 3669 3434 ext. 3098
E-mail: juanmanuel@iteso.mx

Dr. Gerardo Romo L.
Intel
Phone: +5233 3540 6148
E-mail: gerardo.romo@intel.com

CRUCE
COMUNIDAD ITESO>SEMANAL>OCTUBRE 23/06>No.325

La importancia de la integridad de señales

TEXTO ERNESTO RAYAS *

Con el objetivo de promover la importancia de la integridad de las señales en el diseño electrónico moderno, y difundir el estado del arte en el diseño de interconexiones electrónicas de alta velocidad, el 5 y 6 de octubre se llevó al cabo la Segunda Jornada Internacional ITESO-Intel sobre Integridad de Señales.

La integridad de señales es un campo emergente que algunos consideran ya una especialidad de la ingeniería eléctrica moderna. Se puede definir como el conjunto de métodos y técnicas de ingeniería que buscan asegurar la transmisión y recepción confiable de datos a alta velocidad y sin contaminar el espectro electromagnético. Puede decirse que la integridad de señales se ubica en la intersección de otros campos más tradicionales, como la ingeniería de radio frecuencia y microonda, la teoría electromagnética, la electrónica analógica, el diseño físico, las telecomunicaciones y el diseño digital.

A la actividad asistieron algunos de los más destacados investigadores de universidades como de centros de investigación industrial (http://wsi.iteso.mx/) a nivel mundial, así como de algunas compañías. Se discutieron trabajos de investigación de frontera y se realizaron presentaciones introductorias y tutoriales para los que apenas incursionan en este campo. El ITESO contribuyó con la presentación de un trabajo de investigación que se realiza en el Grupo de Investigación en Ingeniería Asistida por Computadora de Circuitos y Sistemas (www.desi.iteso.mx/caecas/), en el cual participan estudiantes de la Maestría en Diseño Electrónico.

Esta jornada forma parte de un proyecto que el Departamento de Electrónica, Sistemas e Informática mantiene en colaboración con el Centro de Diseño de Intel Guadalajara, en el cual se incluyen componentes de docencia e investigación. Como consecuencia, el ITESO impartió de enero a mayo el primer curso curricular que se ofrece en México en Integridad de Señales, en el que participaron estudiantes de la Maestría en Diseño Electrónico, así como alumnos de Ingeniería Electrónica (http://iteso.mx/~erayas/sihsi.htm).

* Académico del Departamento de Electrónica, Sistemas e Informática

búsqueda: | mapa del sitio | contáctanos | localización

Miercoles 18, Octubre 2006

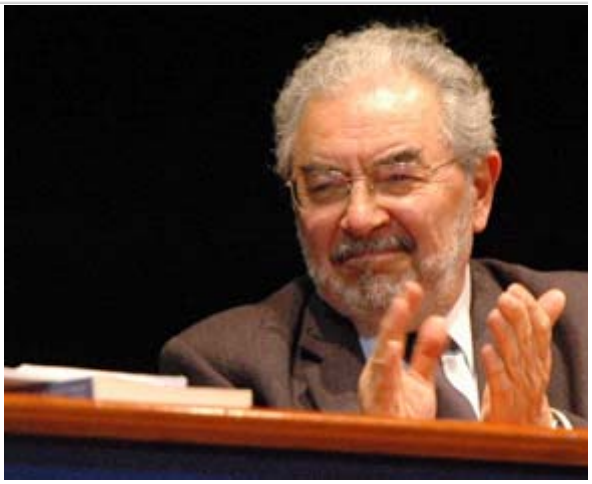
UNIVERSIDAD JESUITA DE GUADALAJARA

ITESO

el ITESO en la
el ITESO en la
el ITESO en la inve
el ITESO en

aspirantes | alumnos | egresados | study at iteso

El ITESO publica libro de presidente de Corte Interamericana de Derechos Humanos



Sergio García Ramírez visitó la Universidad para presentar el texto de su autoría: *Temas de la jurisprudencia interamericana sobre derechos humanos*

MÁS INFORMACIÓN

Los ojos puestos en la animación

Con dos cortometrajes reconocidos fuera de México y una serie que actualmente se transmite en el canal de televisión Cartoon Network, René Castillo, egresado de la carrera de Ciencias de la Comunicación, pretende impulsar la industria de la animación en el país

Expertos discutieron sobre integridad de señales

La Segunda Jornada Internacional sobre Integridad de Señales forma parte de un proyecto educativo que el Departamento de Electrónica, Sistemas e Informática mantiene con el Centro de Diseño de Intel Guadalajara, en el cual se incluyen componentes de docencia e investigación

Tras la promoción de los derechos universitarios

El nuevo procurador de derechos universitarios, Adrián Castañeda, tendrá como una de sus labores continuar con el trabajo que realizaba David López Castillo

MÁS NOTICIAS

licenciaturas

Examen de admisión
Próxima aplicación de examen de admisión el sábado 21 de octubre

Contáctanos

posgrados

Maestría en Comunicación de la Ciencia y la Cultura
Conferencia
"Comunicación de la ciencia"
Impartida por: Maestro Carlos Enrique Orozco
jueves 19 de octubre,
Auditorio A, 19:30 hrs
Entrada libre

Confirmar Asistencia

educación continua

Próxima apertura del diplomado **Dirección**
jueves 19 de octubre

Contáctanos

Próxima apertura del diplomado **Finanzas básicas**
viernes 20 de octubre

Contáctanos

CORREO ITESO

Usuario

ENTRA

ZONA RESERVA

Expediente

ENTRA

¿OLVIDASTE TU C

AGENDA ITESO

SERVICIOS EN LI

sobre
vida aca
c
orientación est
organigrama y di
sala de

Noticia

* Buscar noticias por fechas 2006 Octubre

Expertos discutieron sobre integridad de señales

Con el objetivo de promover la importancia de la integridad de las señales en el diseño electrónico moderno, así como difundir el estado del arte en el diseño de interconexiones electrónicas de alta velocidad, el 5 y 6 de octubre se llevó al cabo la Segunda Jornada Internacional ITESO-Intel sobre Integridad de Señales (Second ITESO-Intel International Workshop on Signal Integrity, I3WSI-2006).

La integridad de señales es un campo emergente que algunos consideran ya una especialidad de la ingeniería eléctrica moderna. Se puede definir como el conjunto de métodos y técnicas de ingeniería que buscan asegurar la transmisión y recepción confiable de datos a alta velocidad y sin contaminar el espectro electromagnético. Puede decirse que la integridad de señales se ubica en la intersección de otros campos más tradicionales tales como la ingeniería de radio frecuencia y microonda, la teoría electromagnética, la electrónica analógica, el diseño físico, las telecomunicaciones y el diseño digital.

A la actividad asistieron como conferencistas algunos de los más destacados investigadores a nivel mundial en el campo de la integridad de señales, tanto de universidades como de centros de investigación industrial (http://wsi.iteso.mx/), provenientes de la Universidad de Carleton (Ottawa, Canadá), de la Universidad de Carolina del Sur (Columbus, Estados Unidos), de la Universidad McMaster (Hamilton, Canadá), del Instituto de Postgrado de Oregon (Portland, Estados Unidos), del INAOE (Puebla, México), así como de las compañías Sonnet, Ansoft, Intel Columbia, Intel Arizona, Intel Oregon e Intel Guadalajara. Se discutieron trabajos de investigación de frontera, y también se realizaron presentaciones introductorias y tutoriales para los que apenas incursionan en este campo. El ITESO contribuyó con la presentación de un innovador trabajo de investigación que se realiza en el Grupo de Investigación en Ingeniería Asistida por Computadora de Circuitos y Sistemas (www.desi.iteso.mx/caecas/), en el cual participan estudiantes de la Maestría en Diseño Electrónico.

Esta jornada forma parte de un proyecto educativo de largo aliento que el Departamento de Electrónica, Sistemas e Informática del ITESO mantiene en colaboración con el Centro de Diseño de Intel Guadalajara, en el cual se incluyen componentes de docencia e investigación. Como consecuencia de este proyecto educativo, el ITESO impartió durante el semestre de enero-mayo 2006 el primer curso curricular que se ofrece en México en Integridad de Señales, en el que participaron estudiantes de la Maestría en Diseño Electrónico, así como alumnos de los últimos semestres de la Licenciatura en Ingeniería Electrónica (http://iteso.mx/~erayas/sihsi.htm).

Texto: Ernesto Rayas (académico del Departamento de Electrónica, Sistemas e Informática)

AGENDA ITESO
SERVICIOS EN LI

sobre
vida aca
c
orientación est
organigrama y di
sala de

INSTITUTO TECNOLÓGICO Y DE ESTUDIOS SUPERIO
PERIFÉRICO SUR MANUEL GÓMEZ MORÍ
TLAQUEPAQUE
TÉLEFONO CONMUTADOR ·