

An Introduction to APLAC

Dr. José Ernesto Rayas-Sánchez

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APLAC Simulator

- APLAC was originally developed at the Technical University of Helsinki, Finland
 - It was originally commercialized by APLAC Solutions Corp., Finland
- 
- APLAC was later acquired by AWR and embedded in Microwave Office
 - AWR was later acquired by National Instruments (NI)
 - NI was recently acquired by Cadence



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APLAC Simulator (cont.)

- Original version of APLAC:
 - A comprehensive mixed-mode high frequency circuit-based simulation and optimization system
 - It was able to realize EM-based simulation, optimization and design centering
- Current version of APLAC, restricted to circuit simulation (with emphasis on HB), is embedded in Cadence/AWR Design Environment™/Microwave Office

<https://www.awr.com/resource-library/microwave-office-aplac-datasheet>

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APLAC Circuit Analysis Modes

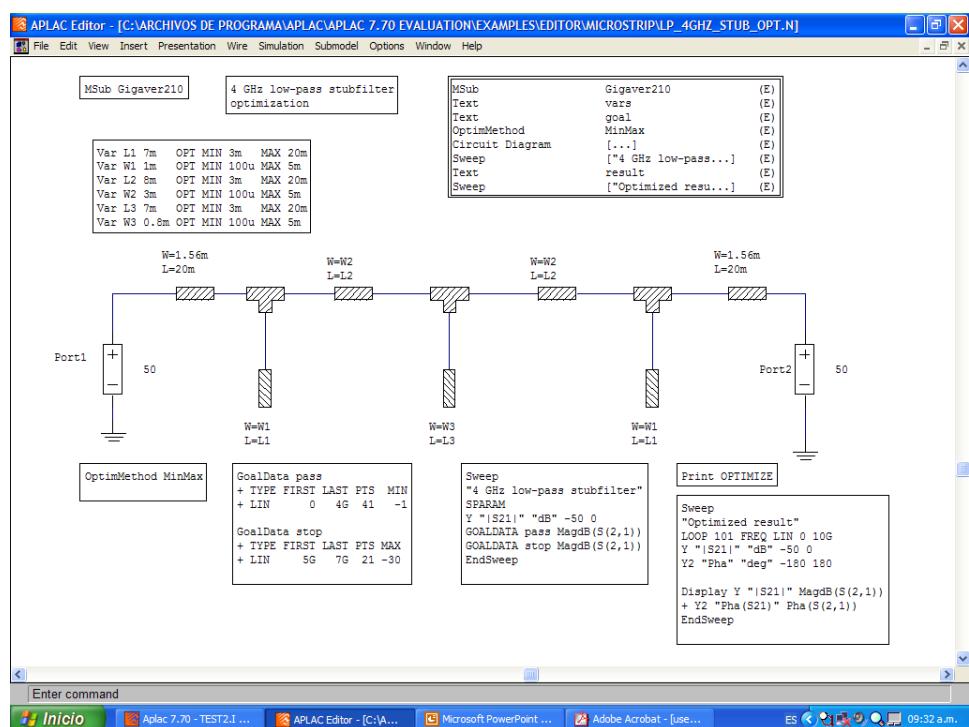
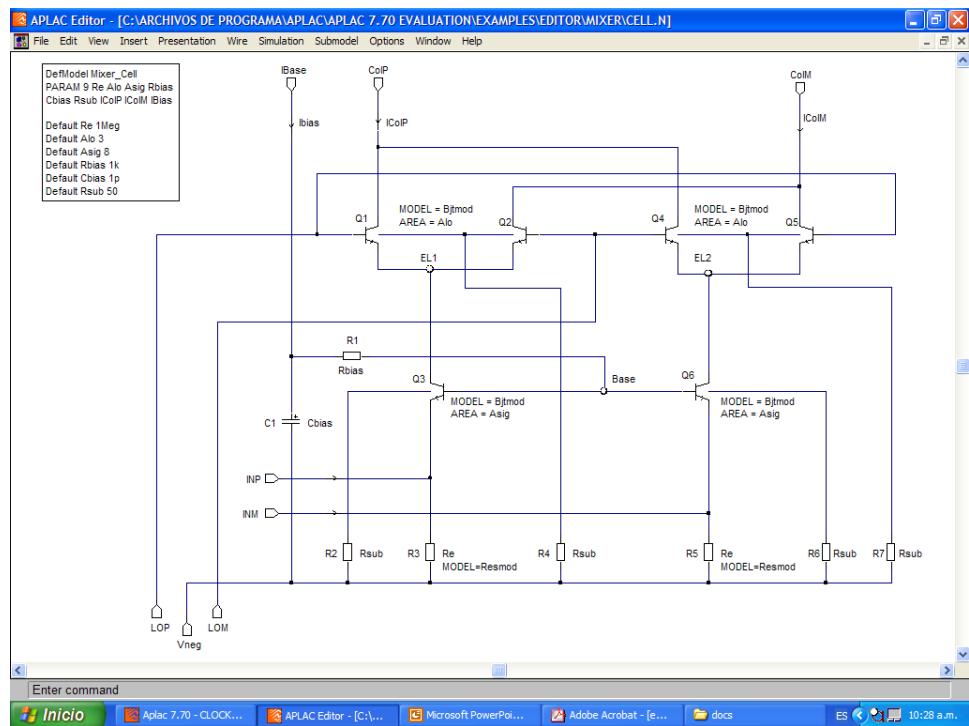
- DC analysis and DC sensitivity
- AC analysis and AC sensitivity
- Transient analysis
- Monte Carlo analysis
- Stability analysis
- Group delay analysis
- S-parameter analysis
- AC Noise analysis
- Harmonic Balance (Single-Multitone, Large Signal)

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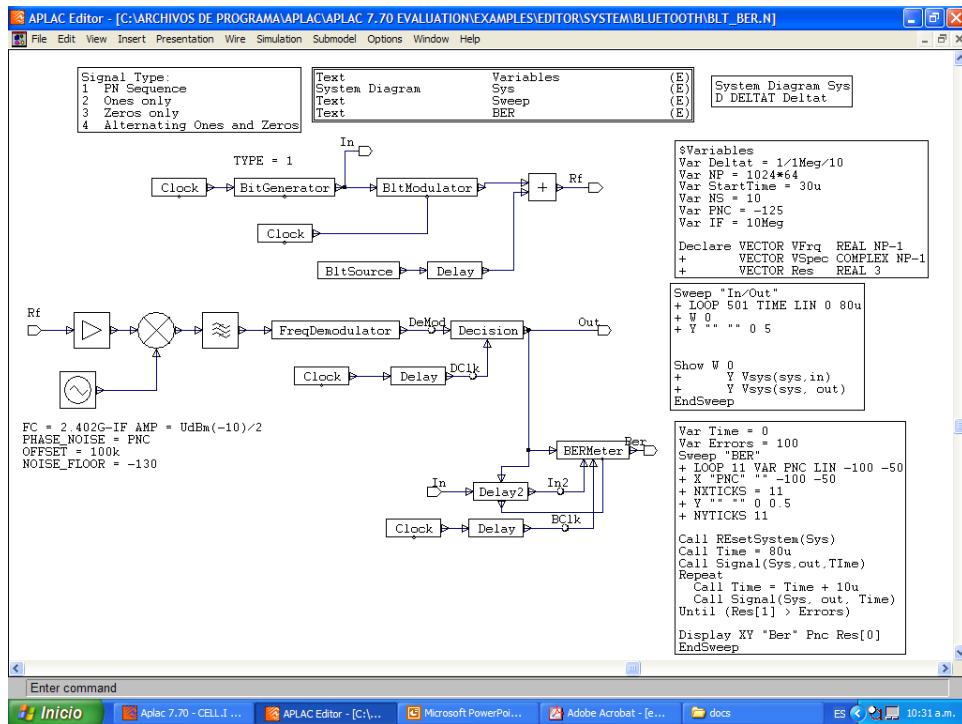
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APLAC Programs

- Aplac Simulator (aplac.exe)
 - Aplac Editor (aplaced.exe)

APLAC Editor

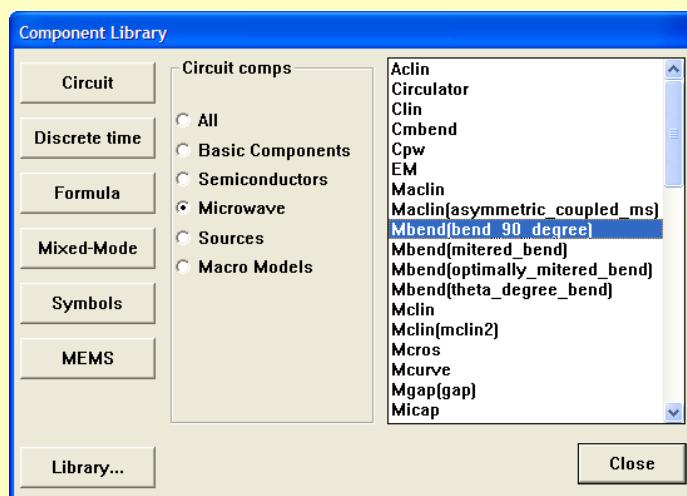
- Diagrams
 - Circuit diagrams
 - System diagrams
- Control objects

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Drawing Schematics

Insert > Component

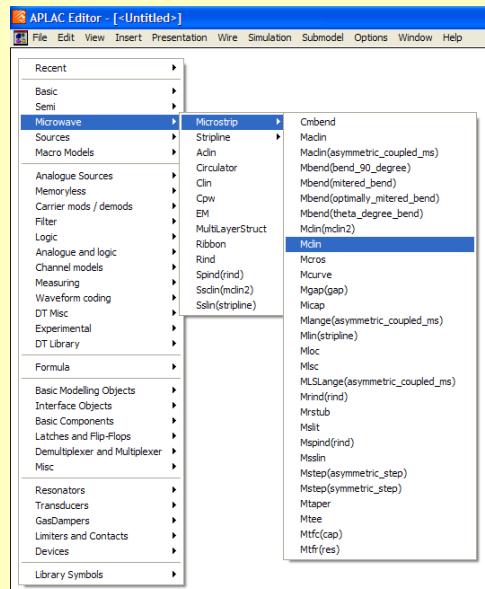


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Drawing Schematics (cont.)

Right click:

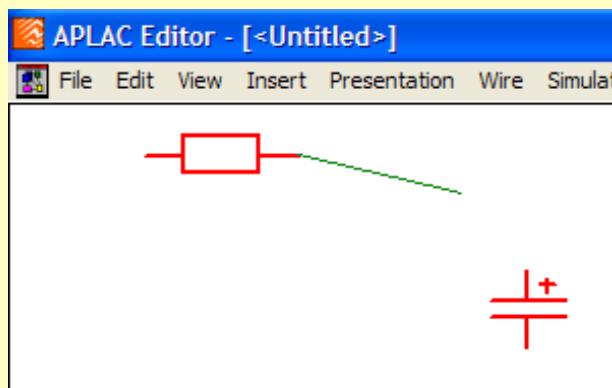


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Drawing Schematics (cont.)

Double click: insert wire

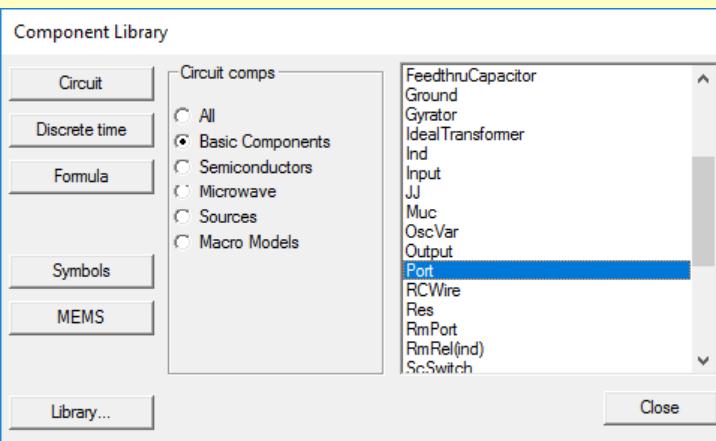


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Drawing Schematics (cont.)

Inserting ports:



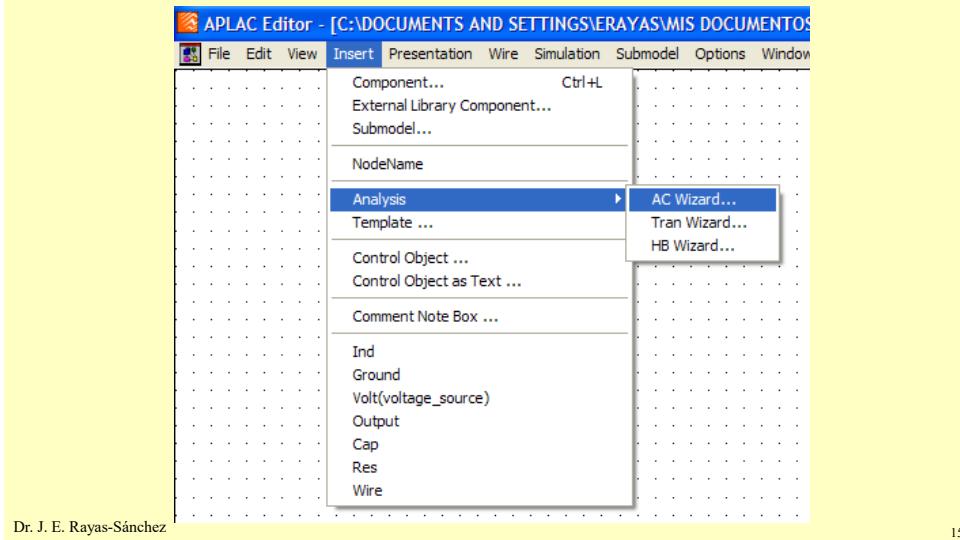
Or... Insert > Port

APLAC Control Objects

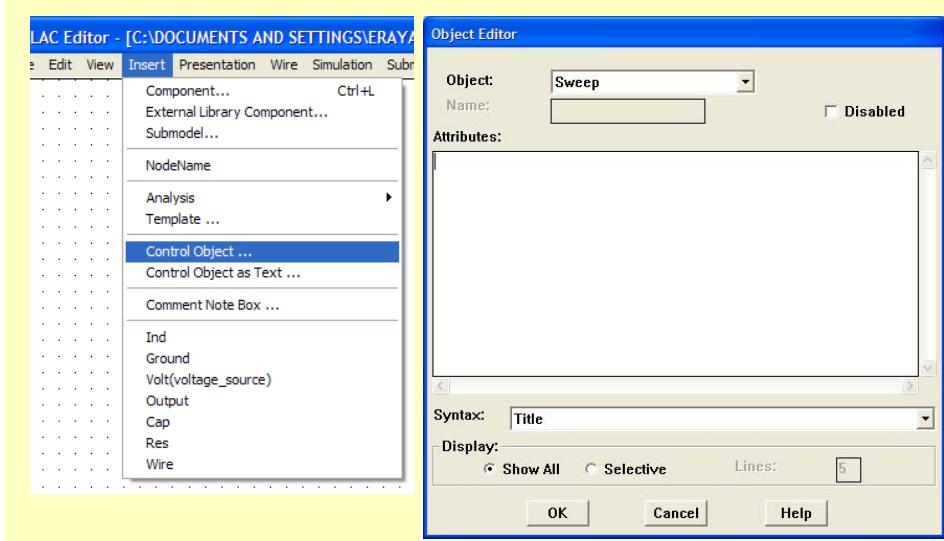
- Using Wizards
- Manually
- Using Analysis Templates

Using Wizards to Setup an Analysis

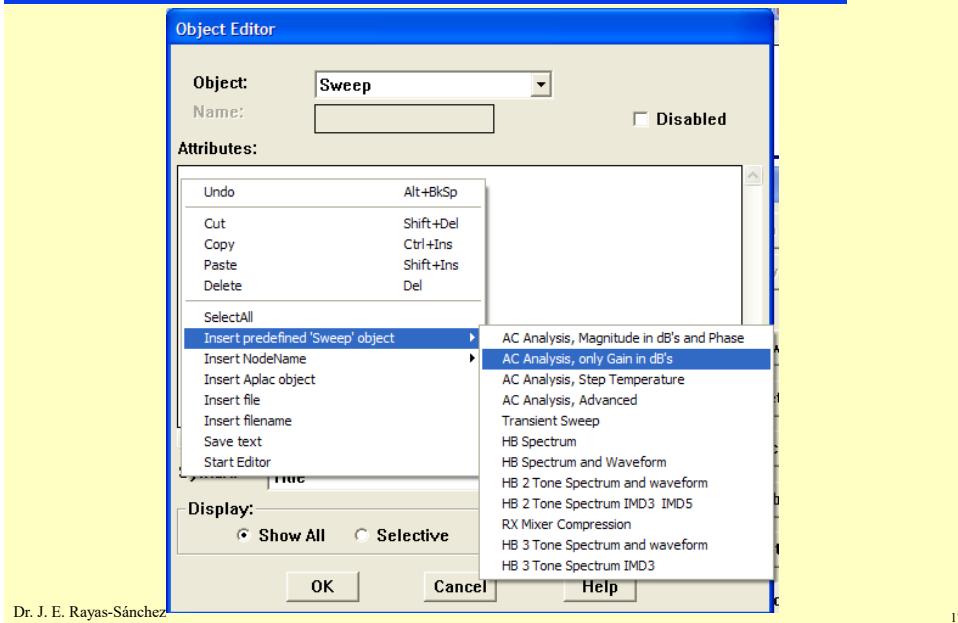
Type of analysis and corresponding sources are easily defined



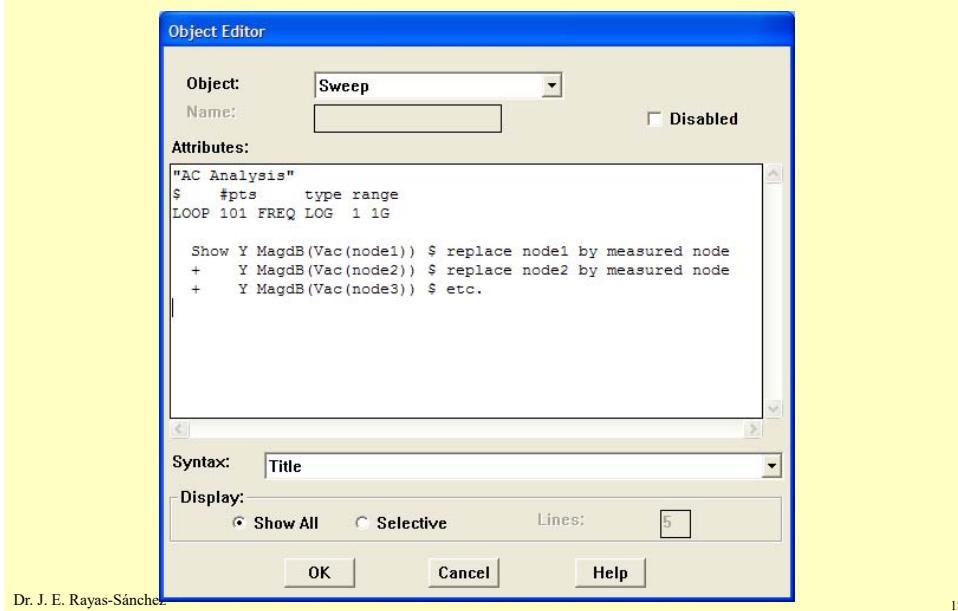
Setting up an Analysis Manually



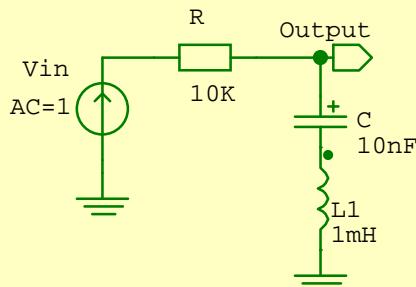
Setting up an Analysis Using Templates



Setting up an Analysis Using Templates (cont.)



A Simple Example

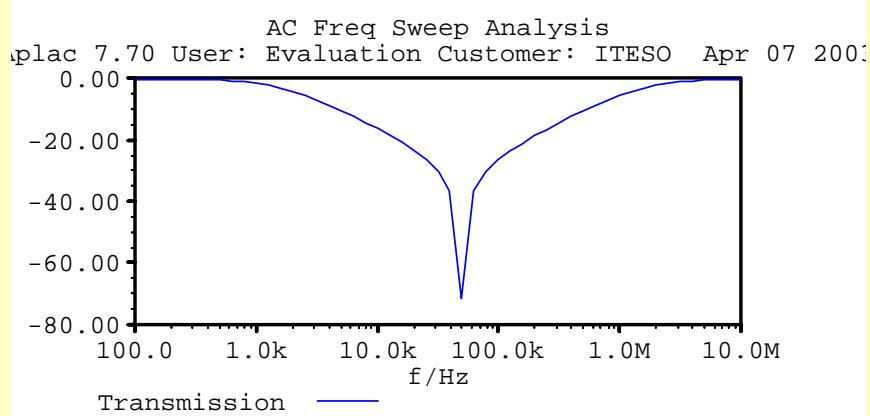


```
$ -----
$ File   : C:\APLAC\PROJECTS\TEST2.I
$ Schema file : C:\APLAC\PROJECTS\TEST2.N
$ Generated with APLAC Editor version 2.7.1
$ Mon Apr 07 09:12:42 2003
$ -----
Res R node1 Output
+ 10K
Cap C Output node2
+ 10nF
Volt Vin node1 GND
+ AC=1
Ind L1 node2 GND
+ 1mH
Sweep "AC Freq Sweep Analysis"
+ loop 51 freq log 100Hz 10MEGHZ
Display Y "Transmission" MagDB(Vac(output))
EndSweep
```

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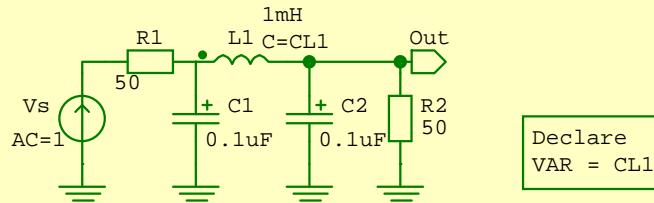
A Simple Example (cont.)



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Declaring and Using Variables

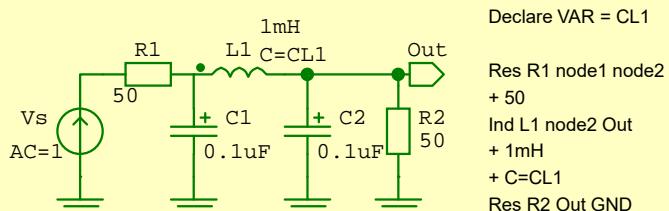


```

Sweep
"AC Filter Gain, for Different Values of CL1"
LOOP 5 VAR CL1 LOG 1p 1n
+ LOOP 10000 FREQ LOG 10Hz 10MEGHZ
Show Y MagdB(Vac(Out))
EndSweep

```

Declaring and Using Variables (cont.)

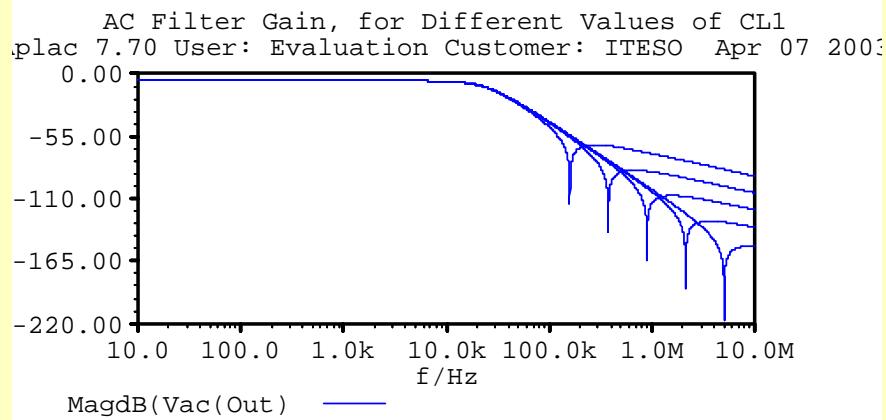


```

Declare VAR = CL1
Res R1 node1 node2
+ 50
Ind L1 node2 Out
+ 1mH
+ C=CL1
Res R2 Out GND
+ 50
Cap C1 node2 GND
+ 0.1uF
Cap C2 Out GND
+ 0.1uF
Volt Vs node1 GND
+ AC=1
Sweep "AC Filter Gain, for Different Values of CL1"
+ LOOP 5 VAR CL1 LOG 1p 1n
+ LOOP 10000 FREQ LOG 10Hz 10MEGHZ
Show Y MagdB(Vac(Out))
EndSweep

```

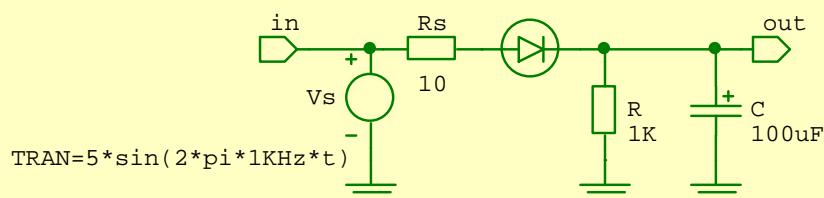
Declaring and Using Variables (cont.)



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Transient Analysis - Example



```
Sweep
"Transient Analysis, Filtered Half-Wave Rectifier"
LOOP 300 TIME LIN 0 15ms

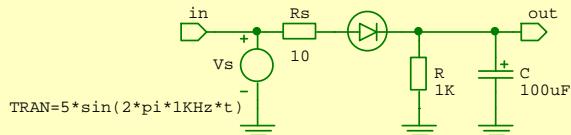
Show Y Vtran(in)
+ Y Vtran(out)

EndSweep
```

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Transient Analysis – Example (cont.)



Res R out GND
+ 1K
Diode D1 node1 out

Volt Vs in GND
+ TRAN=5*sin(2*pi*1KHz*t)
Res Rs in node1
+ 10
Cap C out GND
+ 100uF
Sweep "Transient Analysis, Filtered Half-Wave Rectifier"
+ LOOP 300 TIME LIN 0 15ms
Show Y Vtran(in)
+ Y Vtran(out)

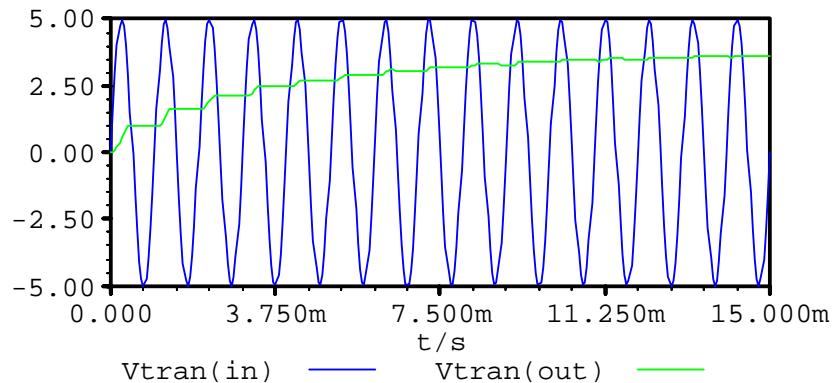
EndSweep

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Transient Analysis – Example (cont.)

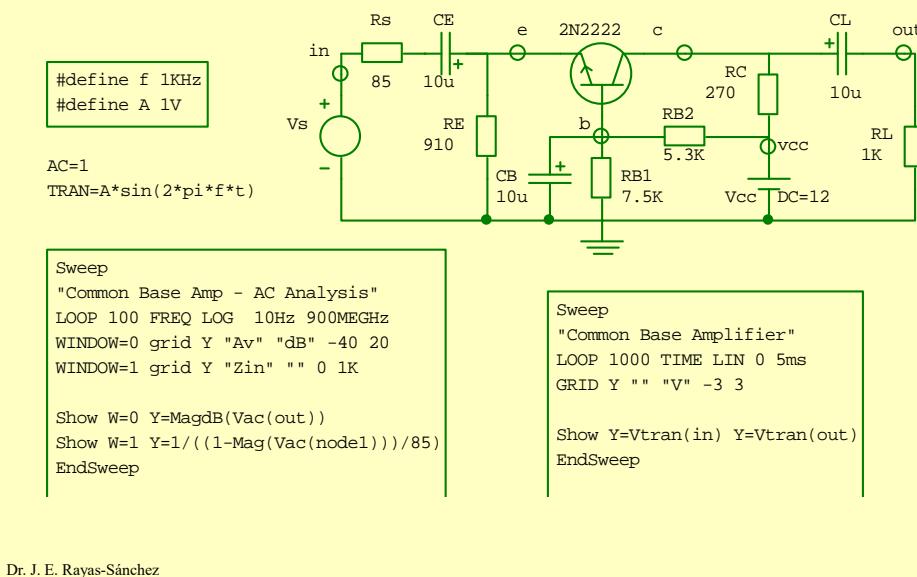
Transient Analysis, Filtered Half-Wave Rectifier
APLAC 8.10 Student version FOR NON-COMMERCIAL USE ONLY



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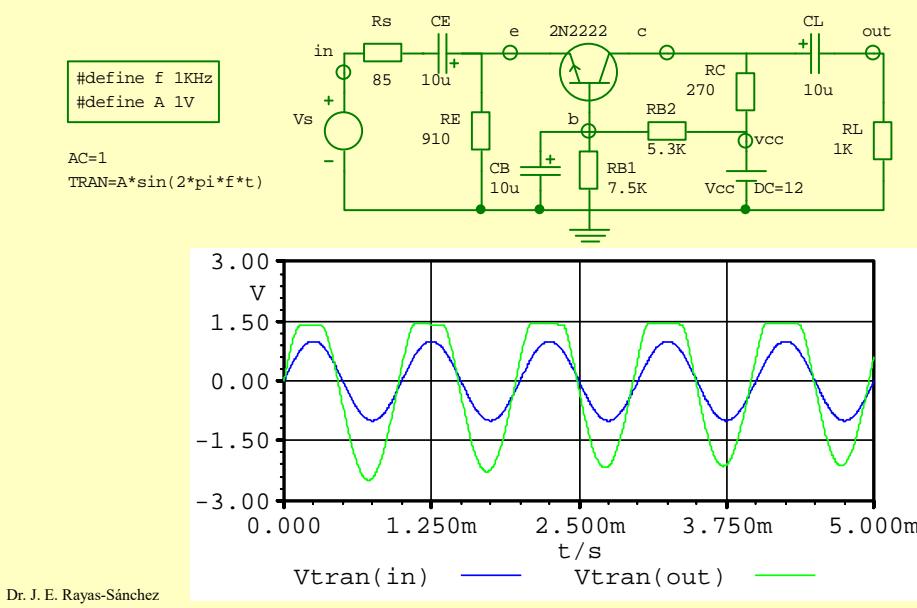
Combining Several Analysis – Example



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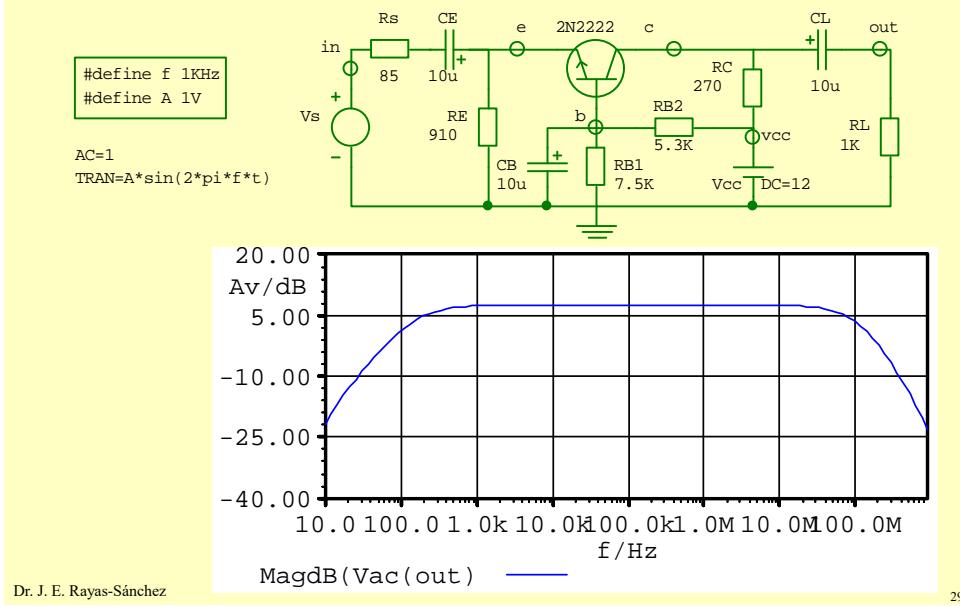
Combining Several Analysis – Example (cont.)



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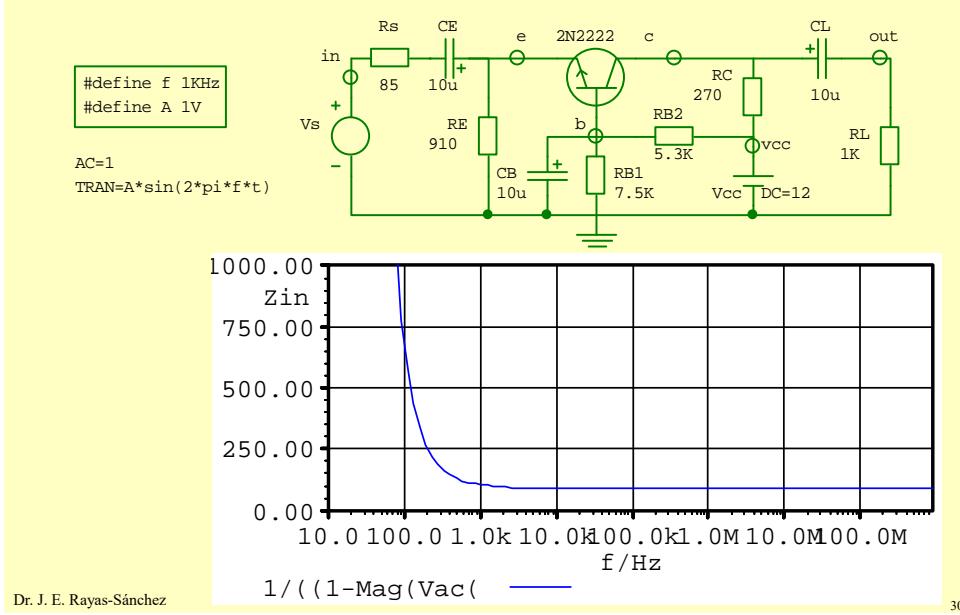
Combining Several Analysis – Example (cont.)



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Combining Several Analysis – Example (cont.)



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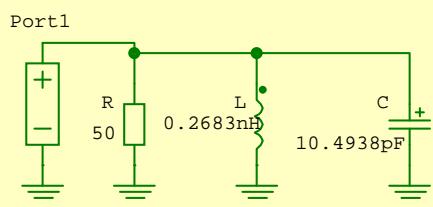
S-Parameter Analysis

- S-parameter analysis (and Y-, Z- and H-parameter analysis as well) is based on the AC analysis
- It is a small signal analysis (for linearized circuits)
- The circuit under simulation must be defined as a multiport network
- In Aplac a multiport is defined with the statement
DefNPort

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S-Parameter Analysis – Example 1



```
Sweep
"S-Parameters Analysis"
LOOP 1000 FREQ LIN 1GHz 5GHz
WINDOW=0 SMITH $ Use Smith Chart
BIGSCREEN

Show W=0 RI=S(1,1) MARKER=1
+ W=1 Y Mag(S(1,1))

EndSweep
```

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S-Parameter Analysis – Example 1 (cont.)

Port1

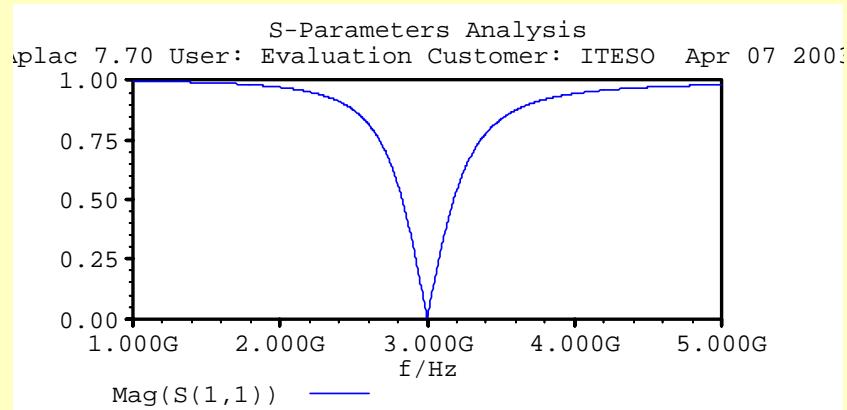
```
Res R Port1 GND
+ 50
Cap C Port1 GND
+ 10.4938pF
Ind L Port1 GND
+ 0.2683nH
DefNPort nport 1
+ Port1 GND 50
Sweep "S-Parameters Analysis"
+ LOOP 1000 FREQ LIN 1GHz 5GHz
+ WINDOW=0 SMITH $ Use Smith Chart
+ BIGSCREEN
Show W=0 RI=S(1,1) MARKER=1
+ W=1 Y Mag(S(1,1))

EndSweep
```

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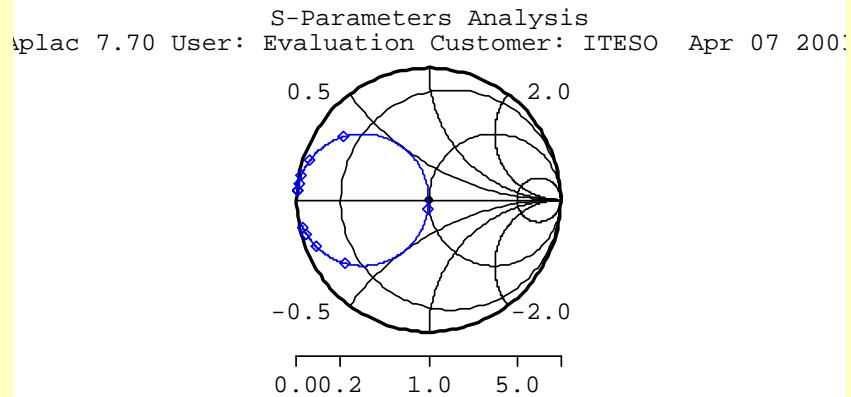
S-Parameter Analysis – Example 1 (cont.)



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S-Parameter Analysis – Example 1 (cont.)

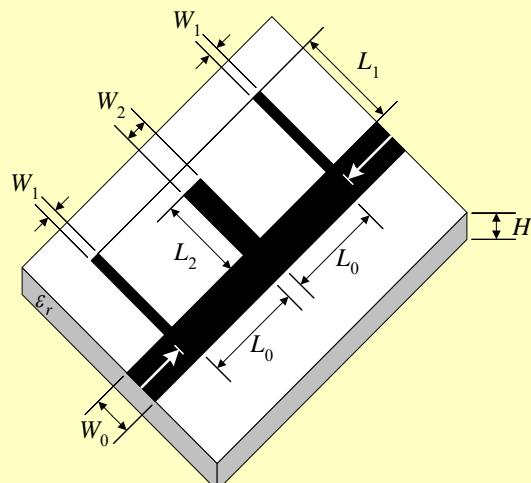


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S-Parameter Analysis – Example 2

Bandstop Microstrip Filter with Quarter-Wave Open Stubs

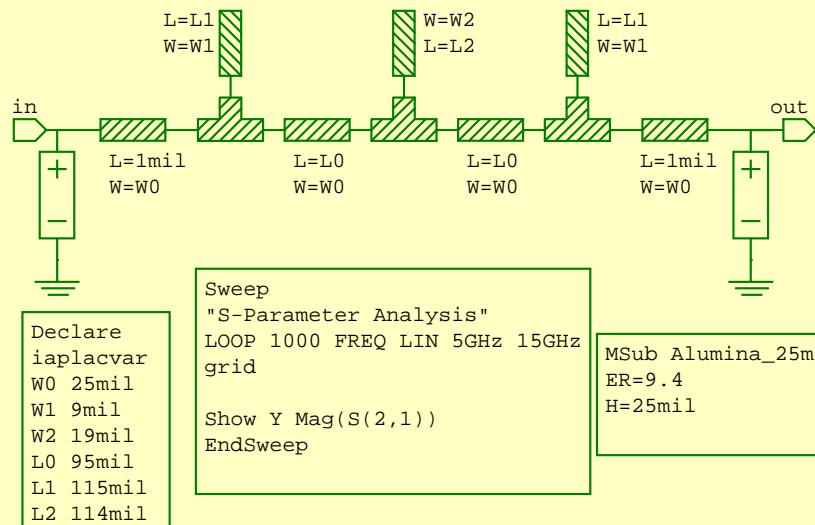


$H = 25$ mil
 $\epsilon_r = 9.4$ (alumina)
 $W_0 = 25$ mil
 $W_1 = 9$ mil
 $W_2 = 19$ mil
 $L_0 = 95$ mil
 $L_1 = 115$ mil
 $L_2 = 114$ mil

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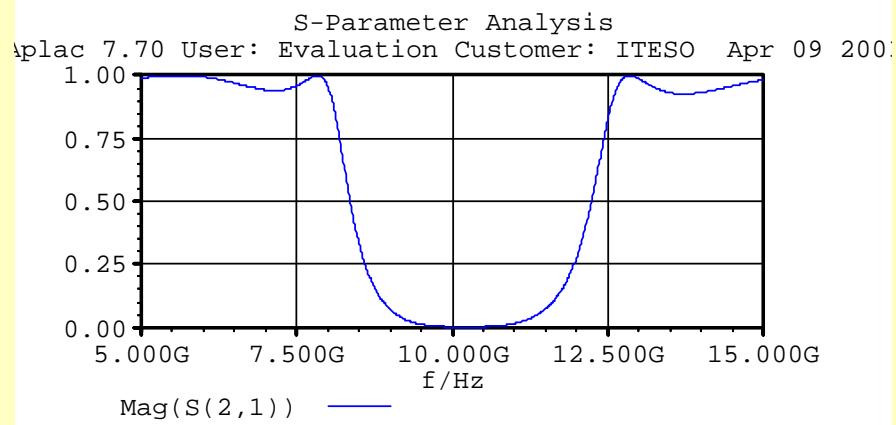
S-Parameter Analysis – Example 2 (cont.)



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S-Parameter Analysis – Example 2 (cont.)



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