

An Improved EM-Based Design Procedure for Single-Layer Substrate Integrated Waveguide Interconnects with Microstrip Transitions

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Outline

- Substrate integrated waveguides (SIW)
- SIW interconnect with microstrip transitions
- Initial design from empirical knowledge
- Direct EM optimization of an SIW surrogate model
- EM simulation of the final structure
- Conclusions

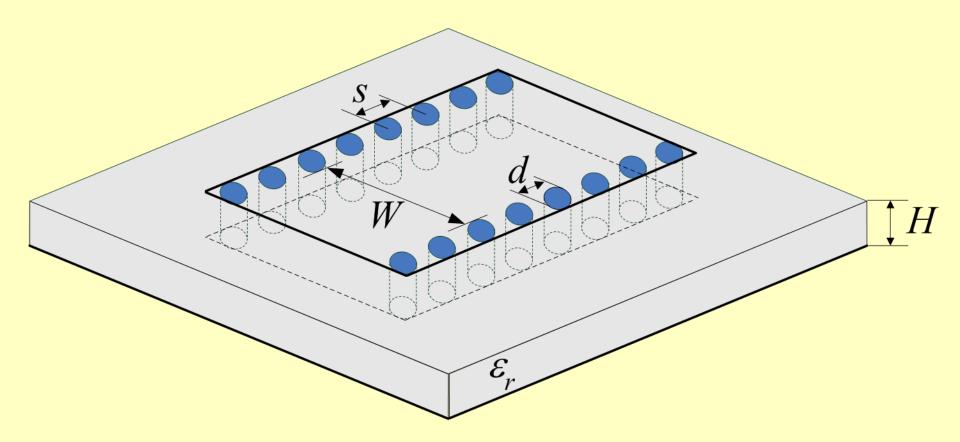


Substrate Integrated Waveguides (SIW)

- SIW structures exploit the advantages of rectangular waveguides and microstrip lines
- They are easy to implement in planar and multilayer structures
- They have low radiation losses and low sensitivity to EMI
- SIW structures are promising candidates for a new generation of low-cost high-speed PCB interconnects



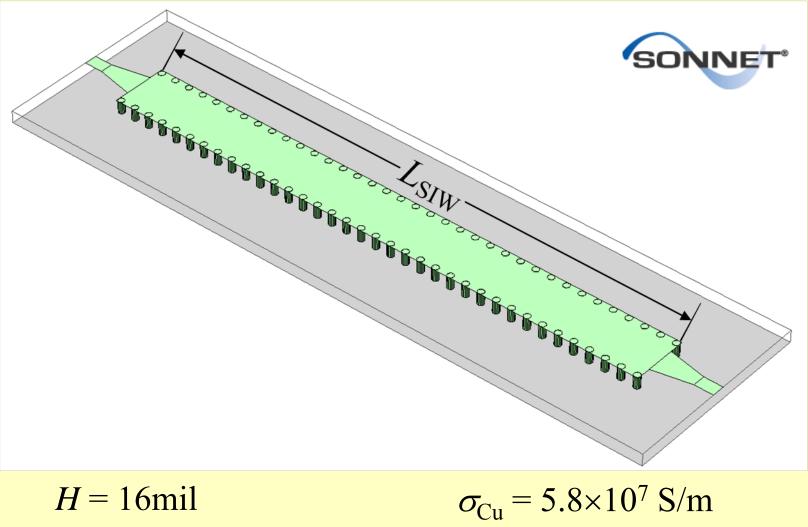
SIW with Vias as Lateral Walls



(Deslandes and Wu, 2001)



SIW with Microstrip Transitions

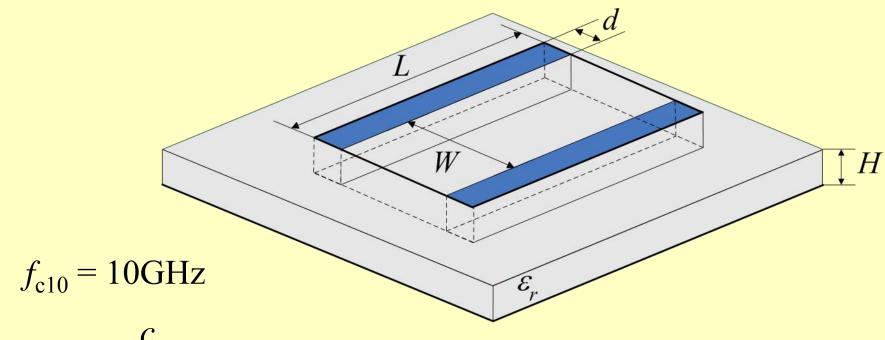


 $\varepsilon_r = 3.6$, tan $\gamma = 0.008$ (Nelco N-4000-13)

t = 0.65 mil



SIW Initial Design



$$W = \frac{c}{2f_{c10}\sqrt{\varepsilon_r}}$$

W = 311.25mil



SIW Initial Design (cont)

To avoid EM leakage,
$$s \le 2d$$

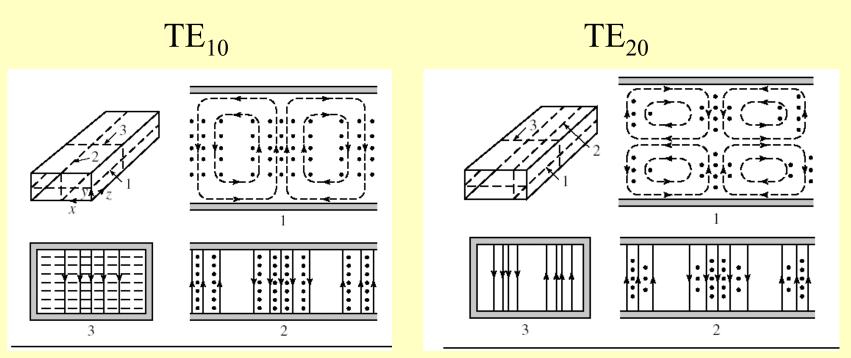
with $d \le \lambda_g/5$ (Deslandes and Wu, 2001)
Using $f_{cmn} = \frac{c}{2\sqrt{\varepsilon_r}} \sqrt{\left(\frac{m}{W}\right)^2 + \left(\frac{n}{H}\right)^2}$ and $\lambda_{g10} = 2\pi / \sqrt{\left(\frac{\varepsilon_r \omega^2}{c^2}\right) - \left(\frac{\pi}{W}\right)^2}$

and considering that the first higher-order mode propagating is the TE_{m0} mode,

 $d \leq \frac{2W}{5\sqrt{m^2-1}}$

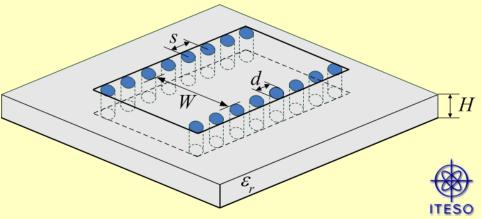
 $d \leq 25.41$ mil (up to TE₅₀ mode)

Only TE Modes Are Supported by SIWs

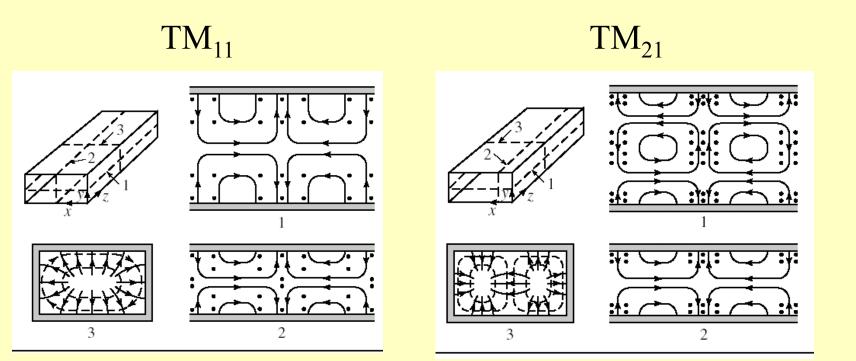


(Pozar, 1998)

Vertical conduction currents flow through the vias

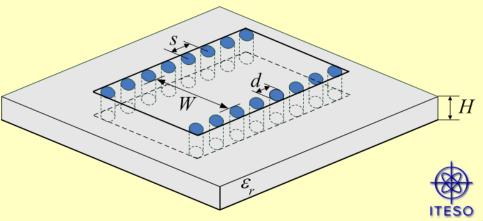


Only TE Modes Are Supported by SIWs (cont)

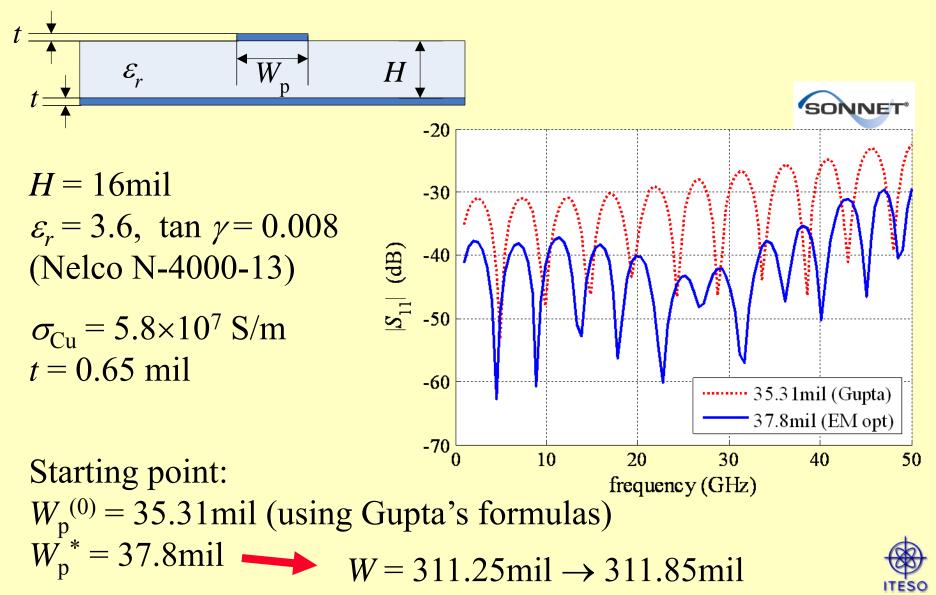


(Pozar, 1998)

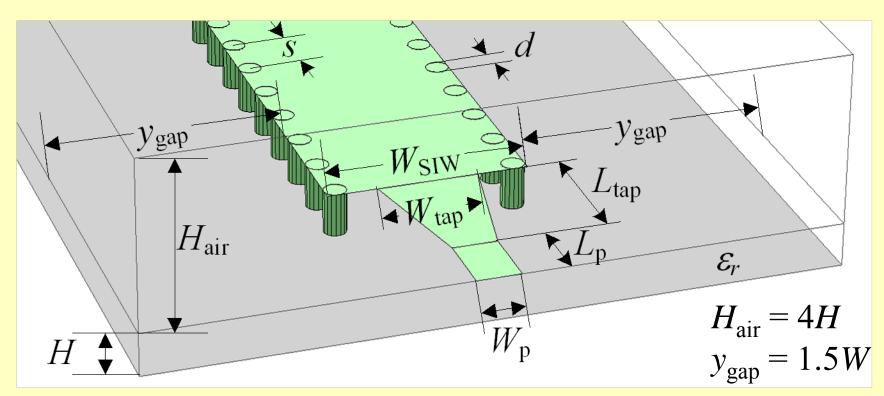
TM modes can not be preserved on SIWs (*Xu and Wu, 2005*)



I/O Microstrip Lines



SIW with Microstrip Transitions – Initial Design

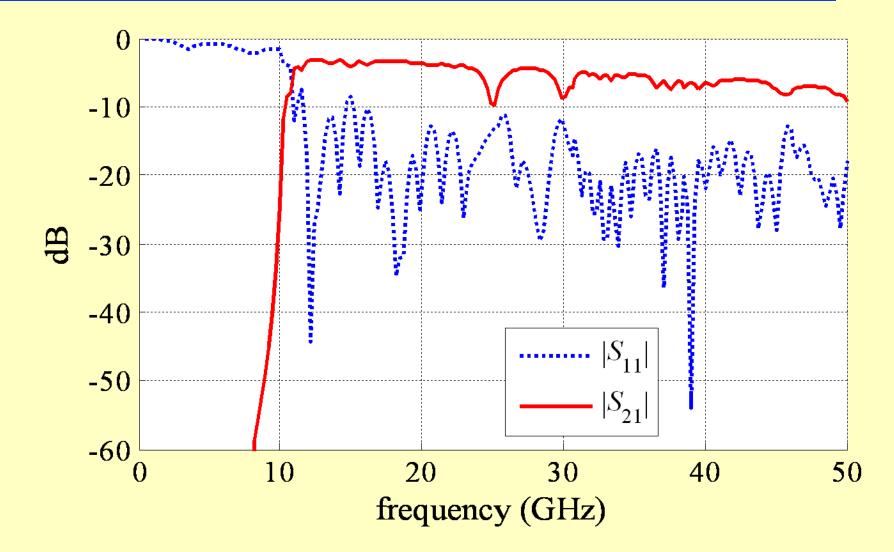


H = 16mil W = 311.85mil $W_p = 37.8$ mil $d = W_p/2 = 18.9$ mil s = 2d $L_{p} = 1.5W$ $L_{tap} = 3W$ $L_{SIW} = 4W$ $W_{SIW} = W + 2d$

Starting point: $W^{(0)} = W$ $W_{tap}^{(0)} = W$



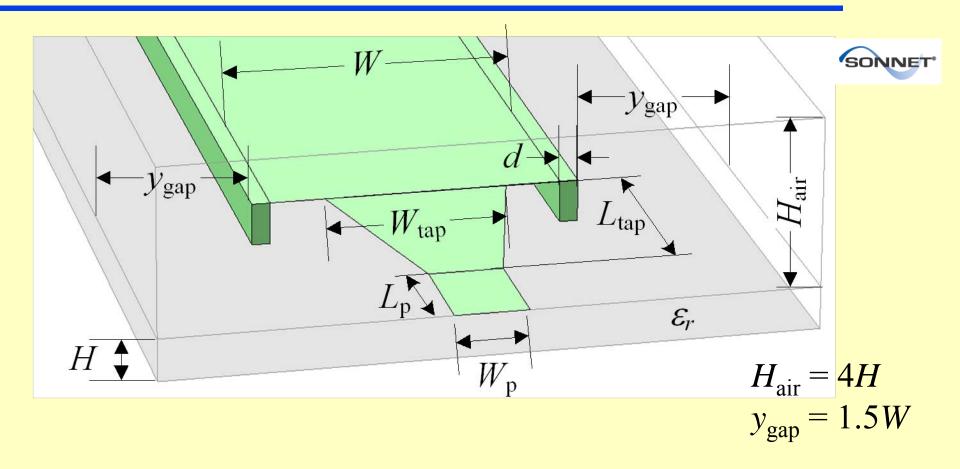
Initial Fine Model Responses



Sim. time: 7 hrs 19 min (CPU 2.16GHz Dual, 2.5GB RAM)



Surrogate Model

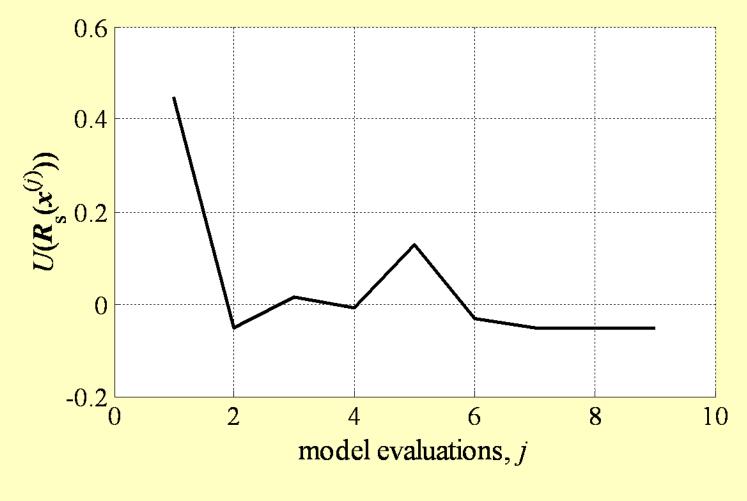


 $C_x = W_p = 37.8 \text{mil} (\lambda/20 = 7.8 \text{mil} \text{ at } 50 \text{GHz})$ where C_x is the cell-size in the longitudinal direction



Optimizing the Low Cutoff Frequency

Surrogate objective function to find W^*

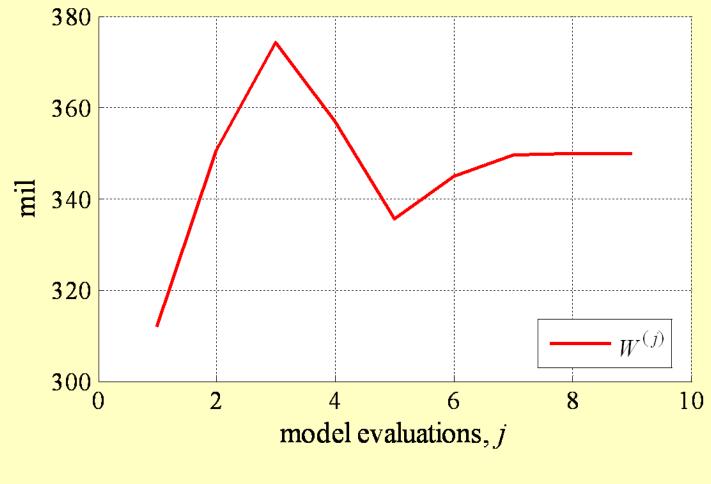


Total optimization time: 3.8 min



Optimizing the Low Cutoff Frequency (cont)

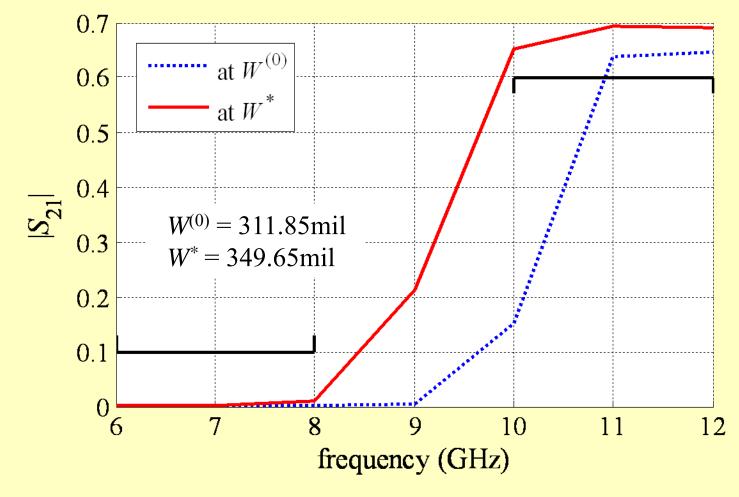
Evolution of *W*



Total optimization time: 3.8 min

Optimizing the Low Cutoff Frequency (cont)

Surrogate responses before and after optimizing *W*

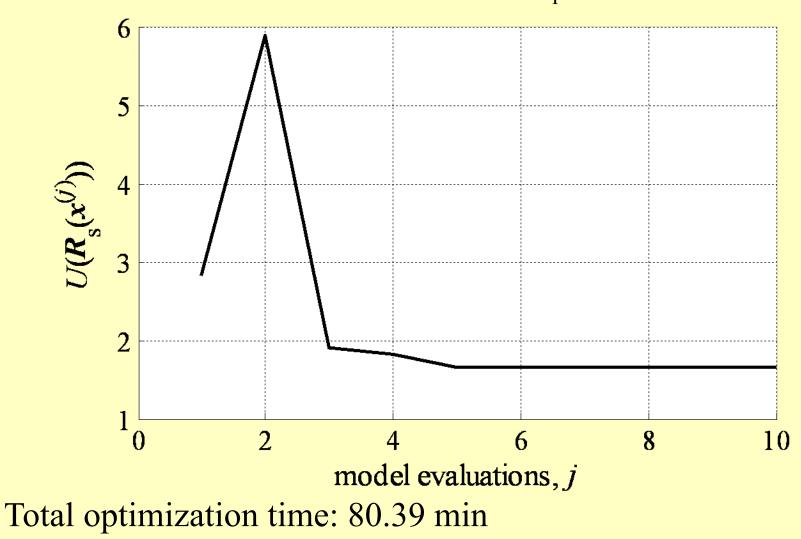


Total optimization time: 3.8 min



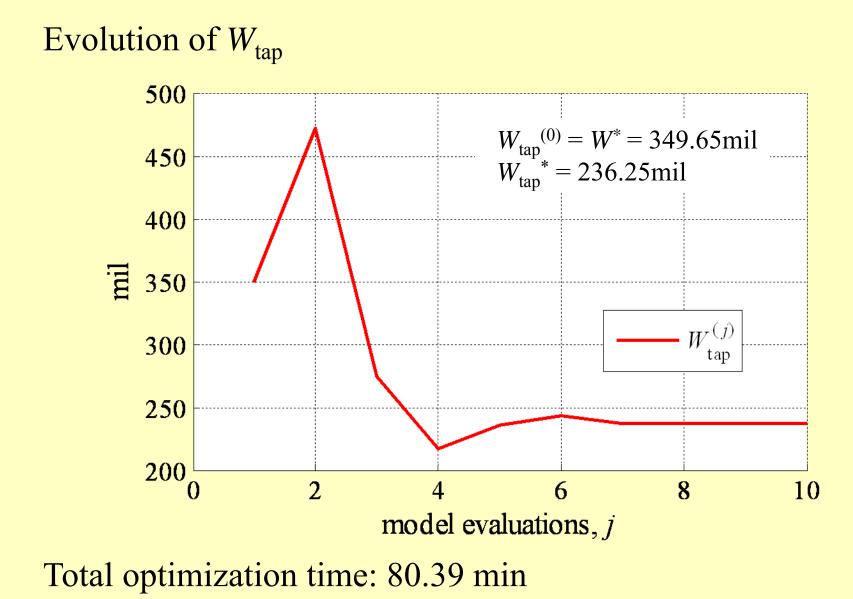
Optimizing the Passband

Surrogate objective function to find W_{tap}^{*}



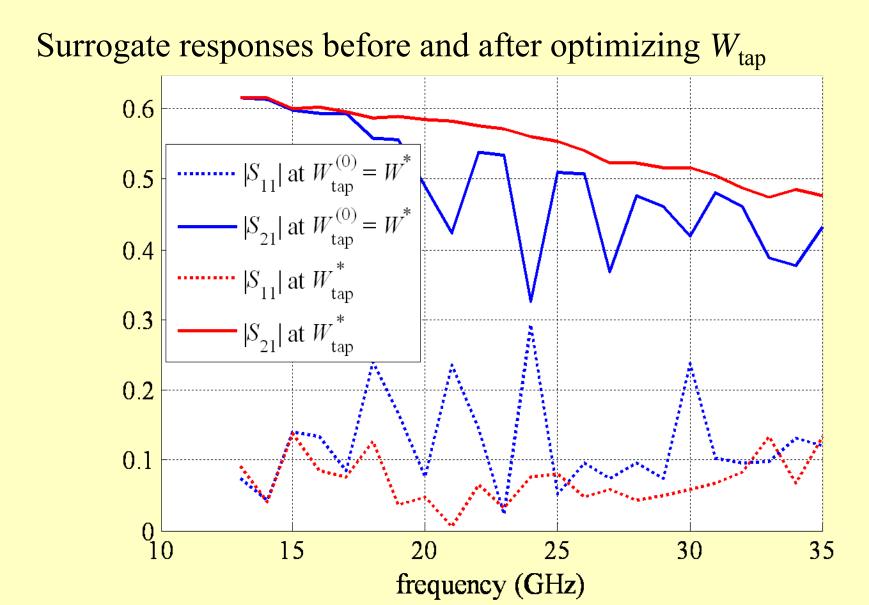
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Optimizing the Passband (cont)



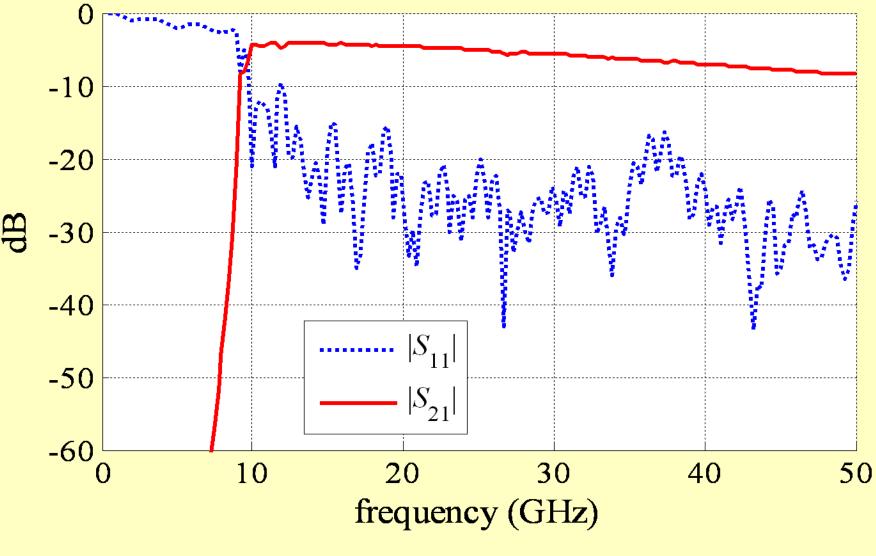


Optimizing the Passband (cont)



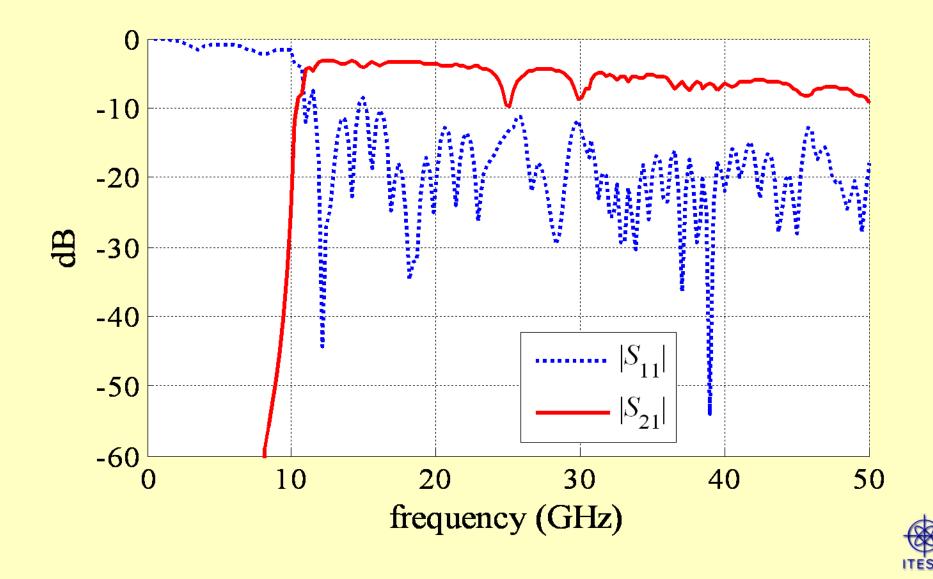
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Final Fine Model Responses

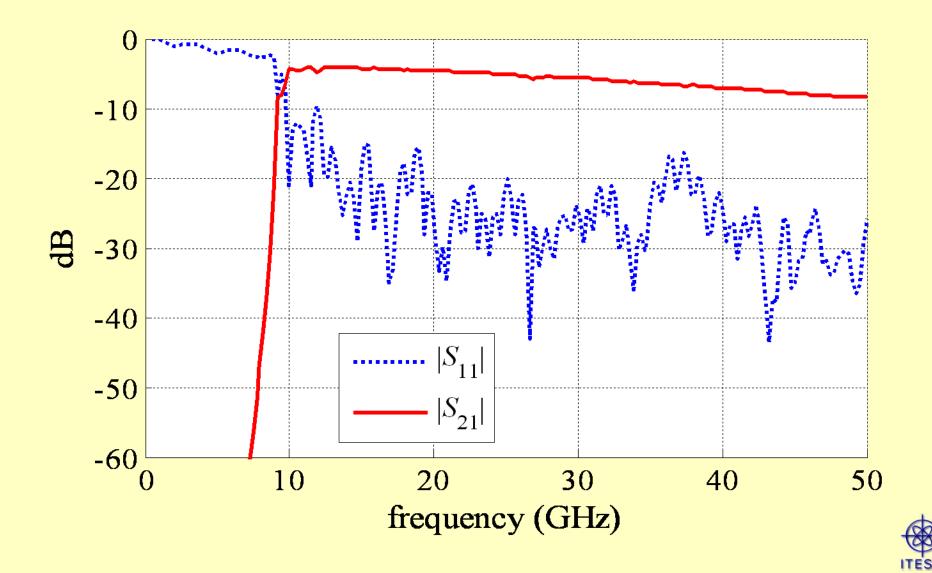


Simulation time: 11 hrs 36 min

Fine Model Responses, Initial



Fine Model Responses, Final



- We described the physical structure of a SIW interconnect with microstrip transitions
- We reviewed a procedure to obtain an initial design, based on empirical knowledge
- We developed a surrogate model for direct inexpensive EM simulation that uses grooves instead of vias
- We optimize the surrogate model in two stages: first optimizing the low cutoff frequency, and second optimizing the transmission and reflections in the passband
- The final fine model exhibits a significantly better performance than the initial design

